

FIG.\_2

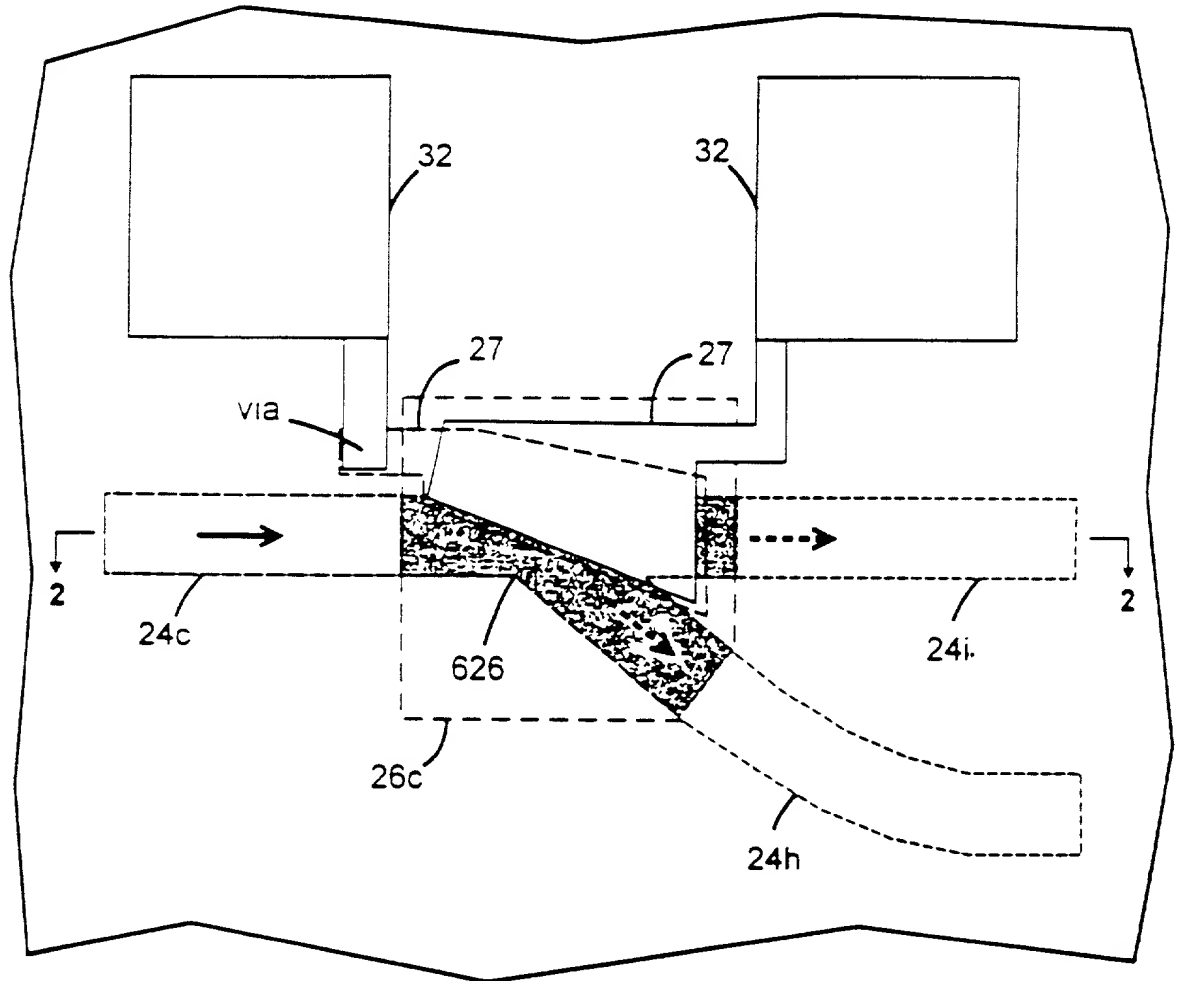


FIG.\_3

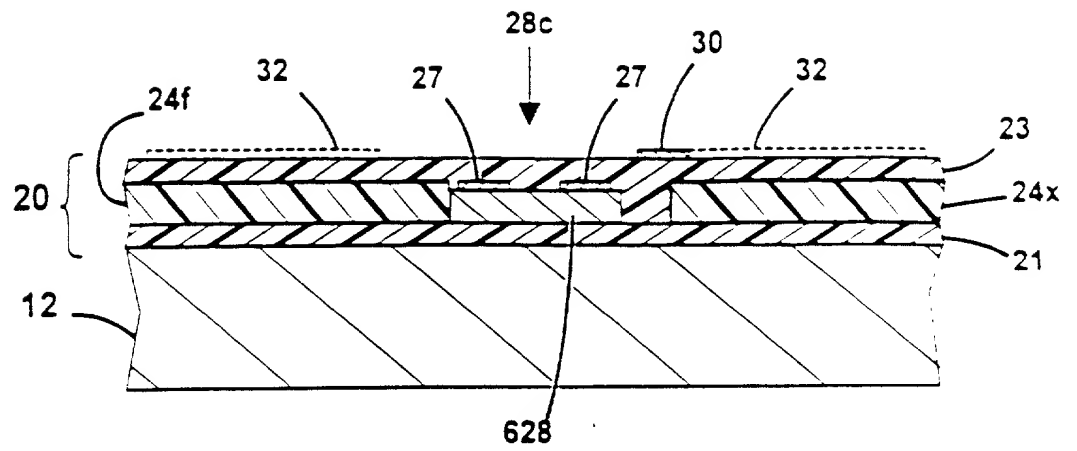


FIG.\_4-1

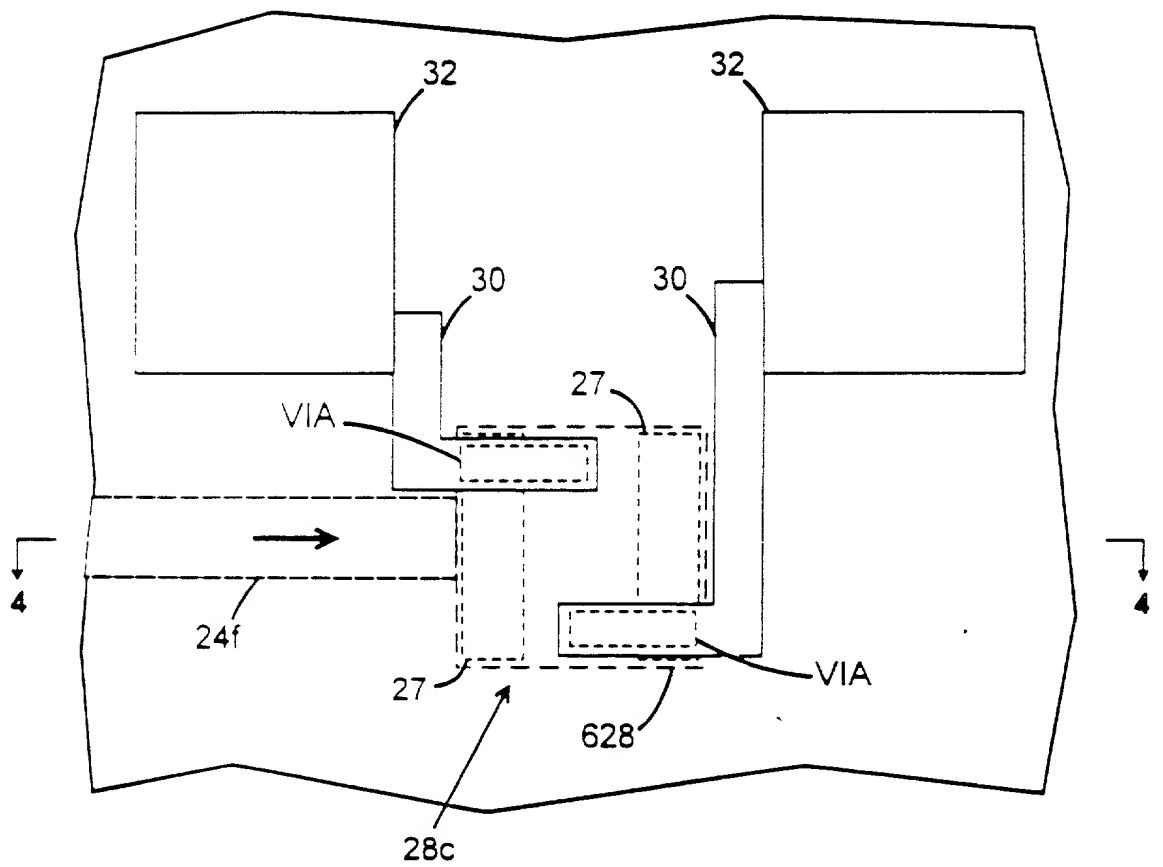


FIG.\_5-1

28c'

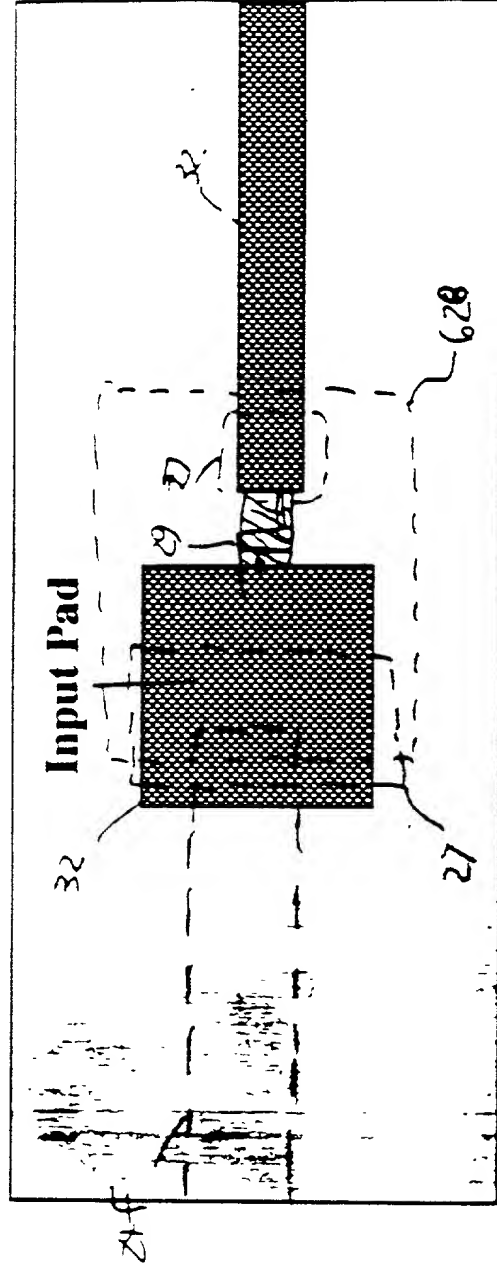


FIG. 5-2

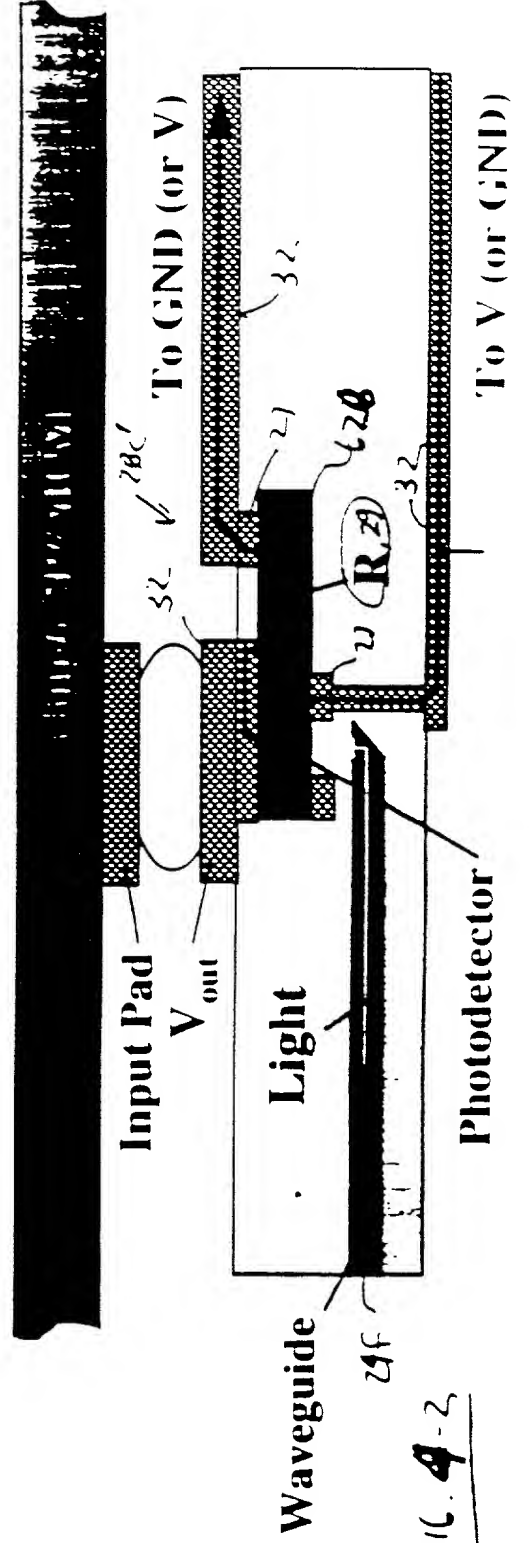


FIG. 4-2



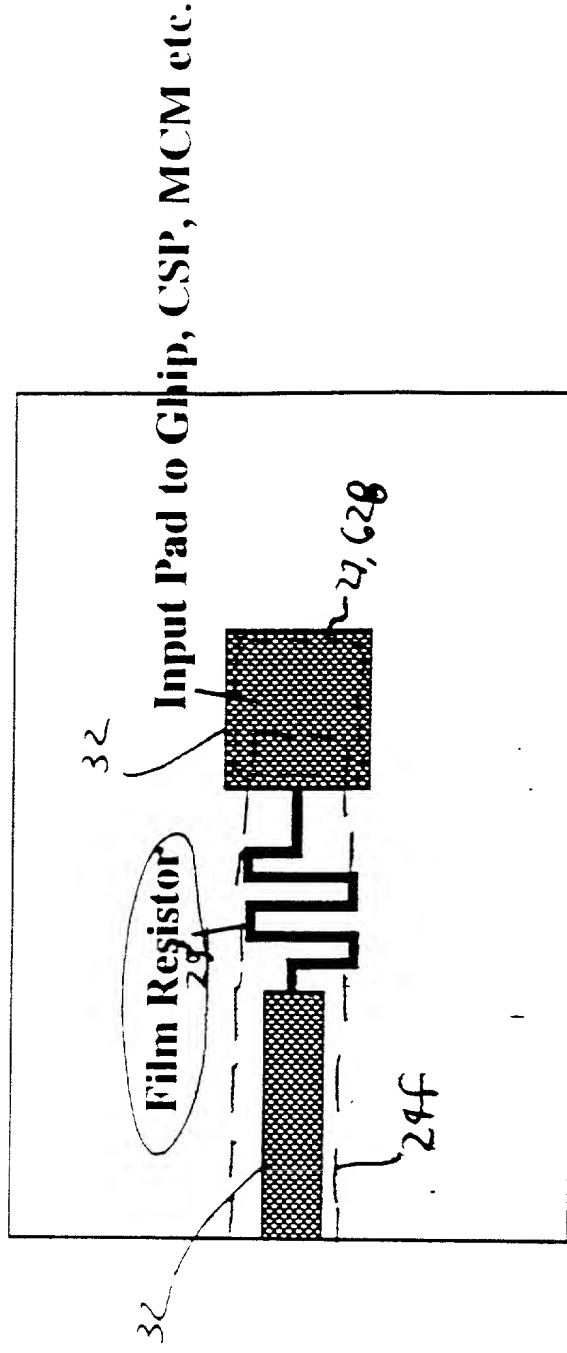


FIG. 5-3

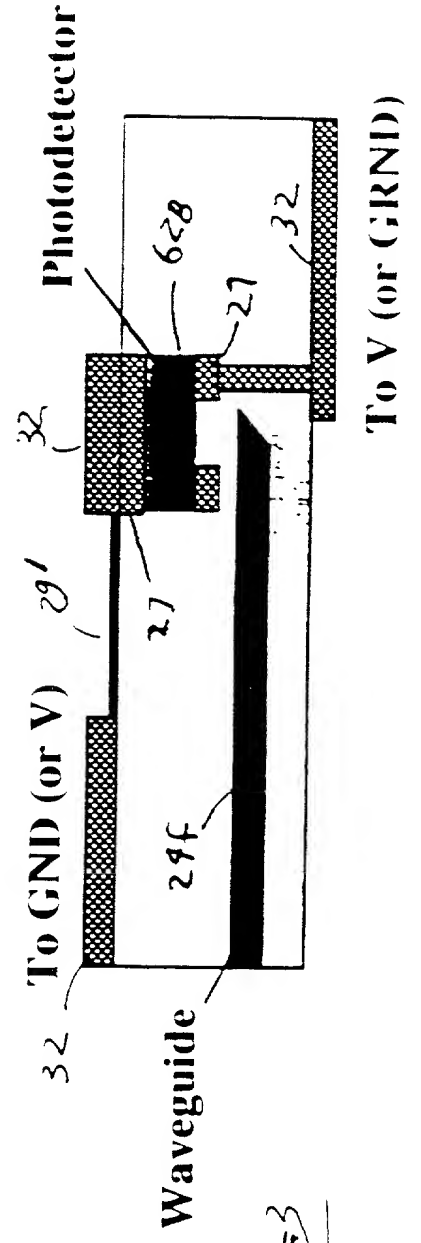


FIG. 4-3

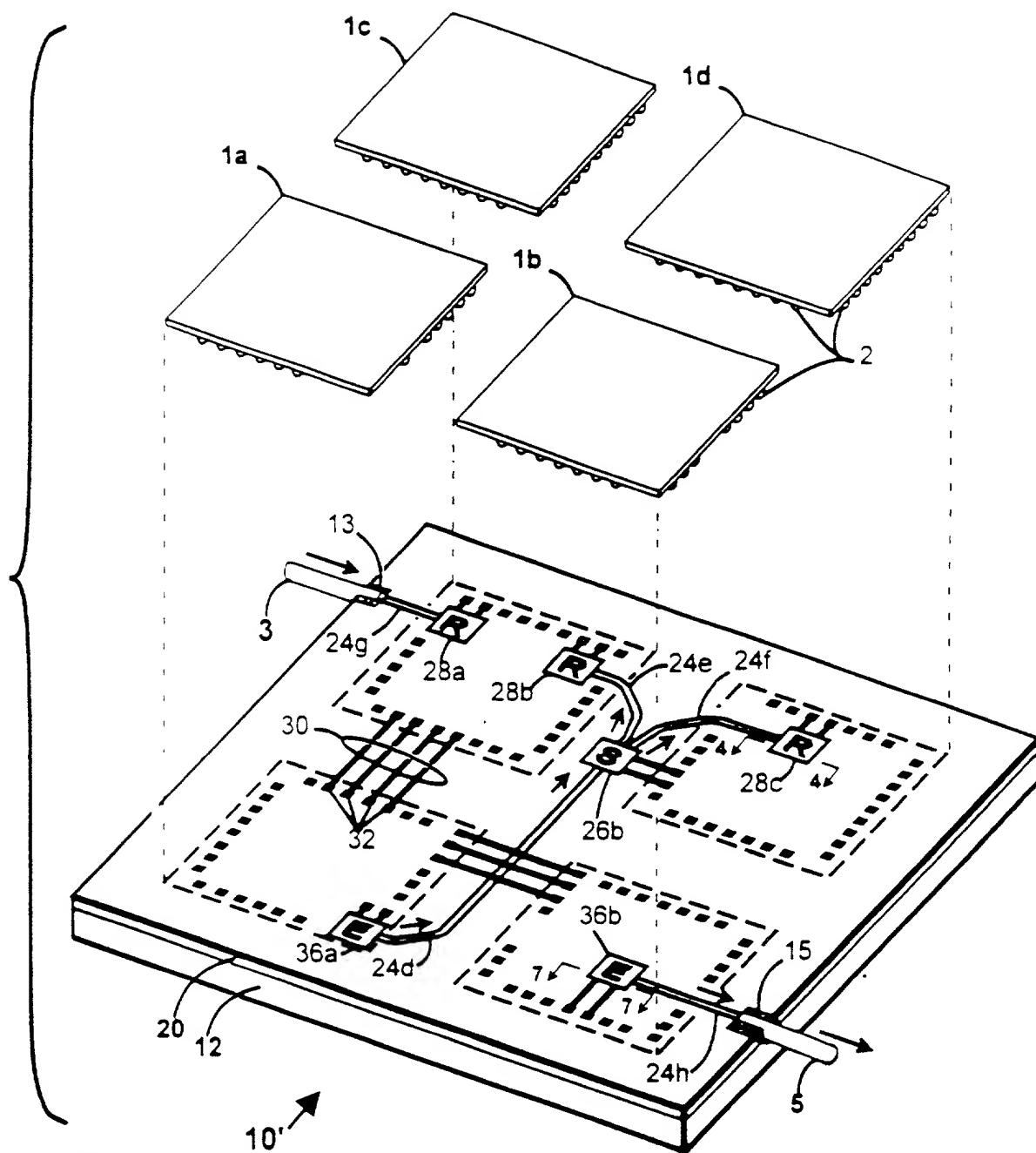


FIG. 6

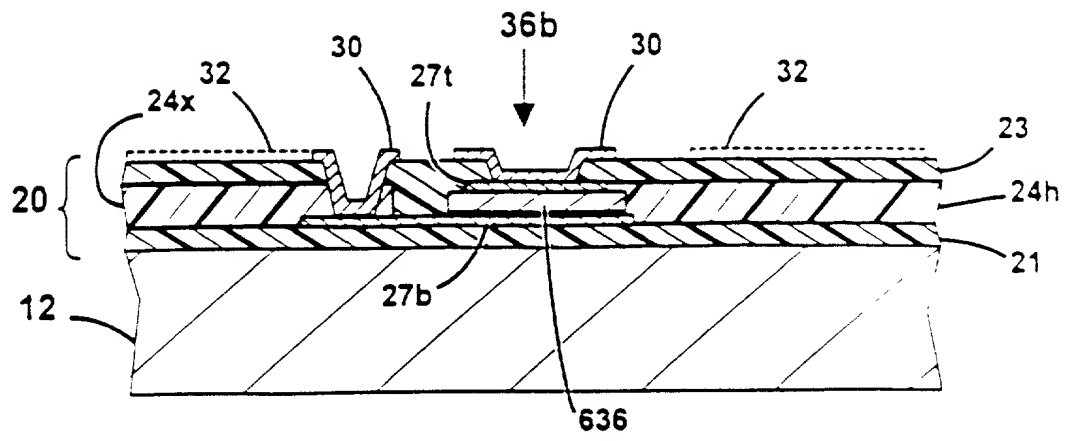


FIG.\_7

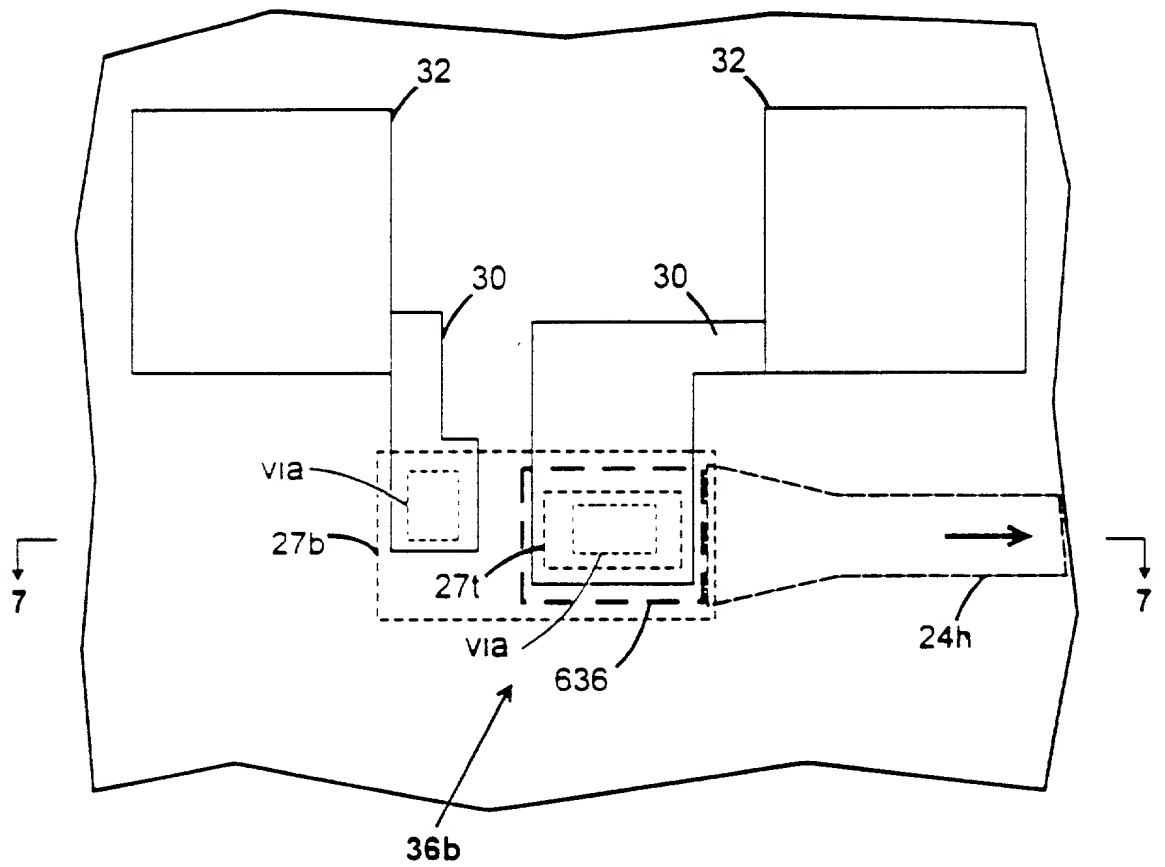
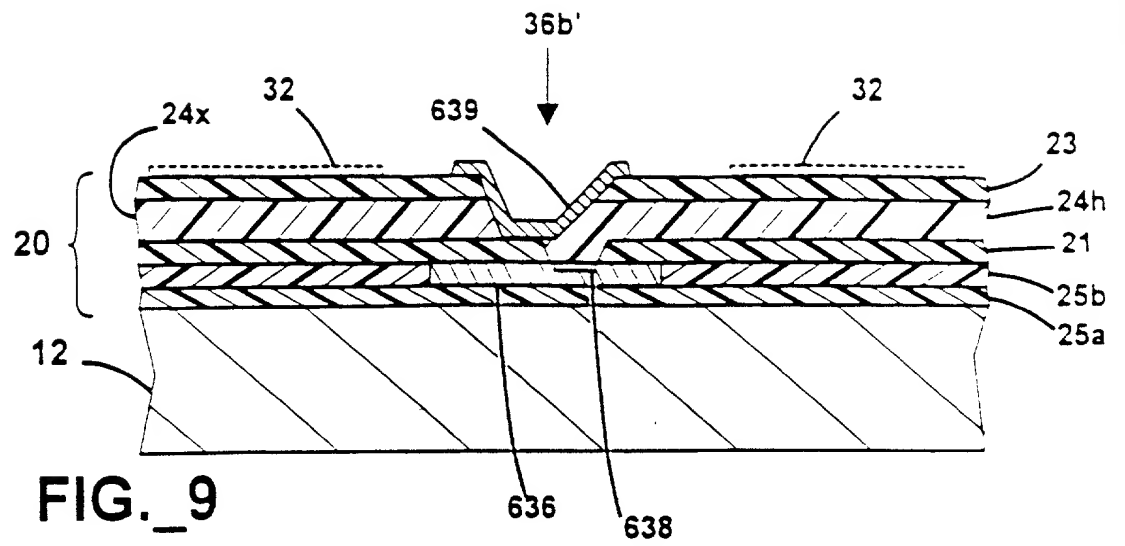
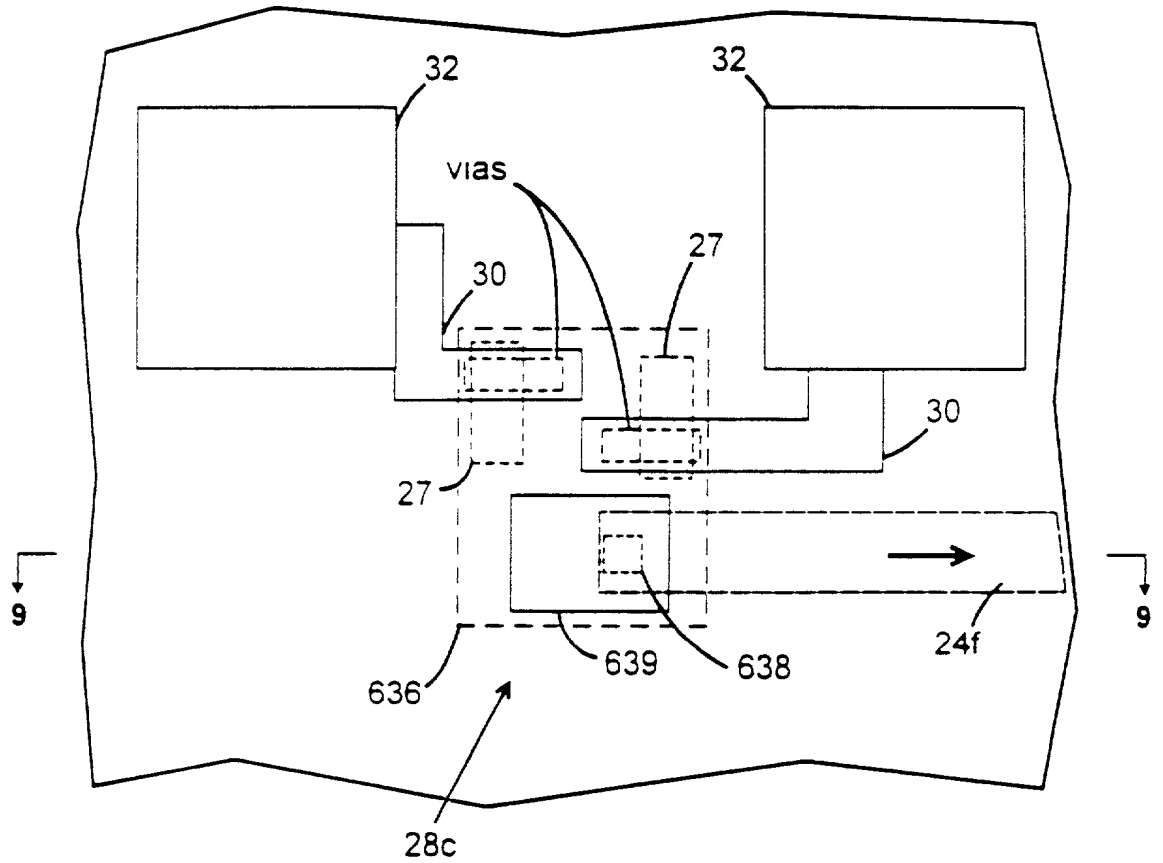


FIG.\_8



**FIG.\_9**



**FIG.\_10**

FIG.\_11

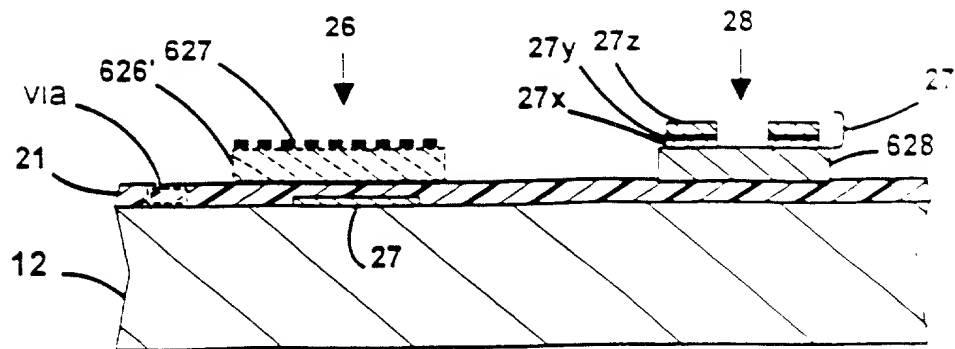


FIG.\_12

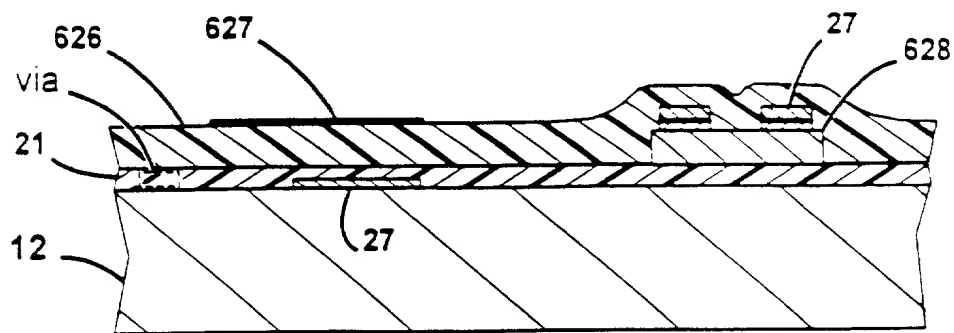


FIG.\_13

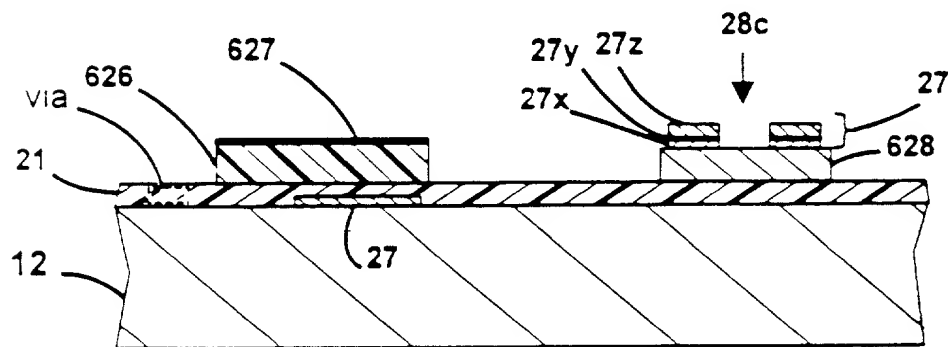
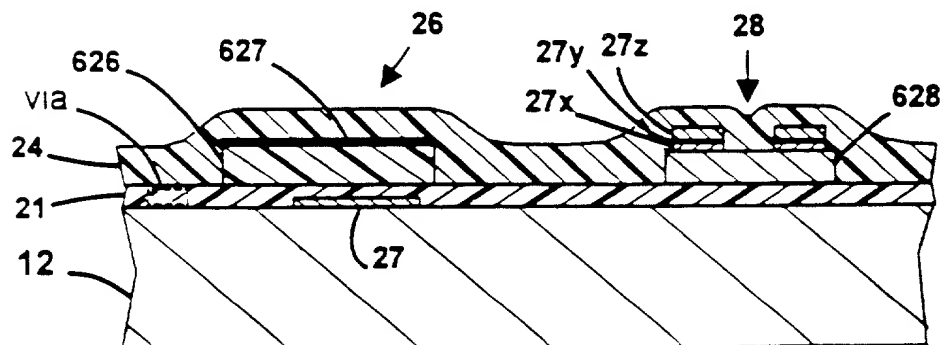


FIG.\_14



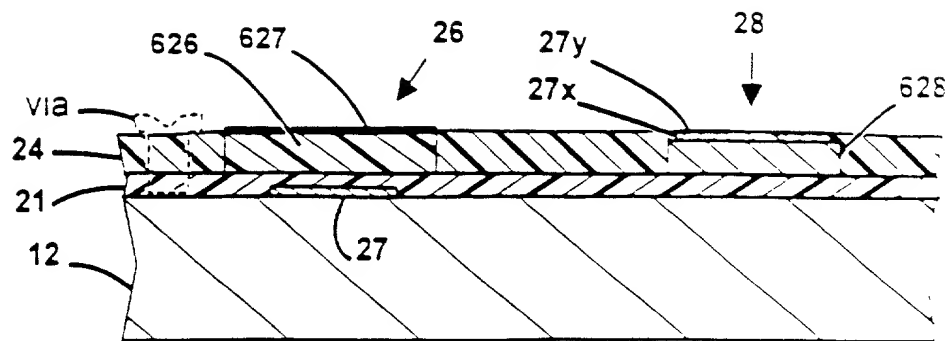


FIG.\_15

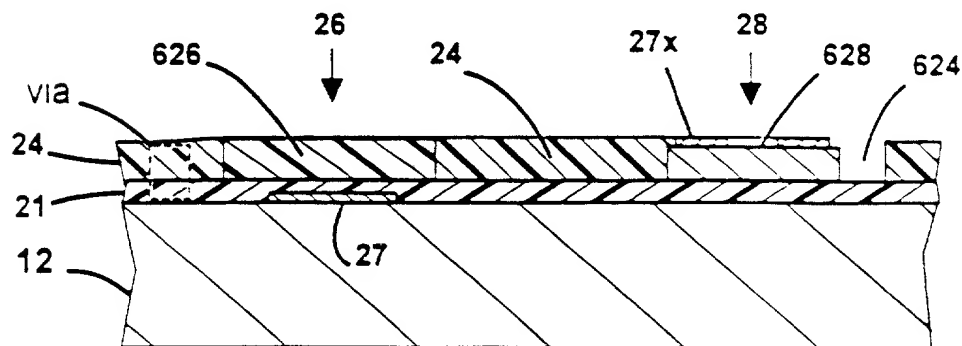


FIG.\_16

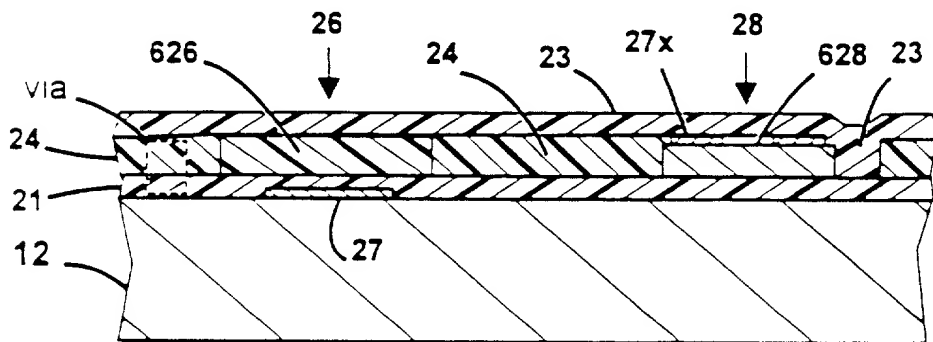


FIG.\_17

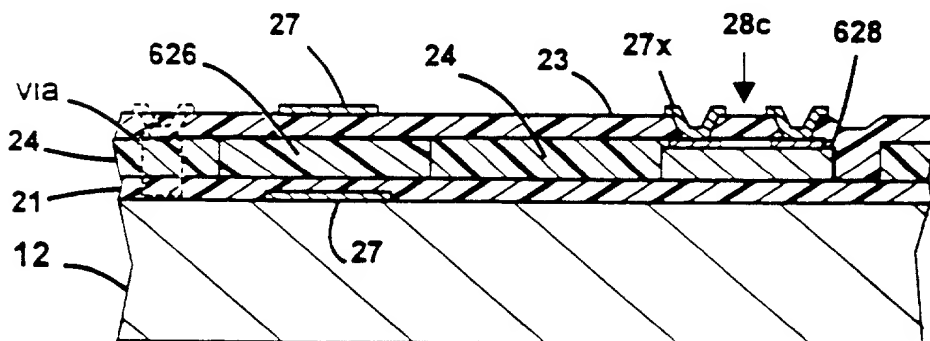


FIG.\_18

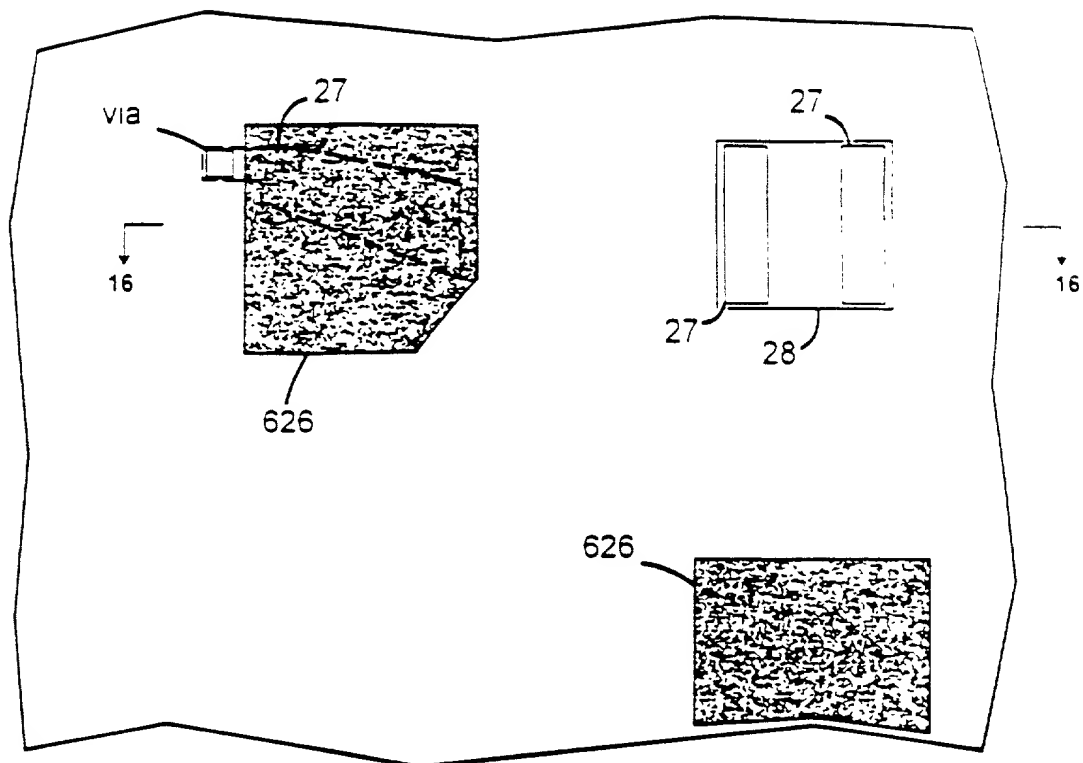


FIG. 19

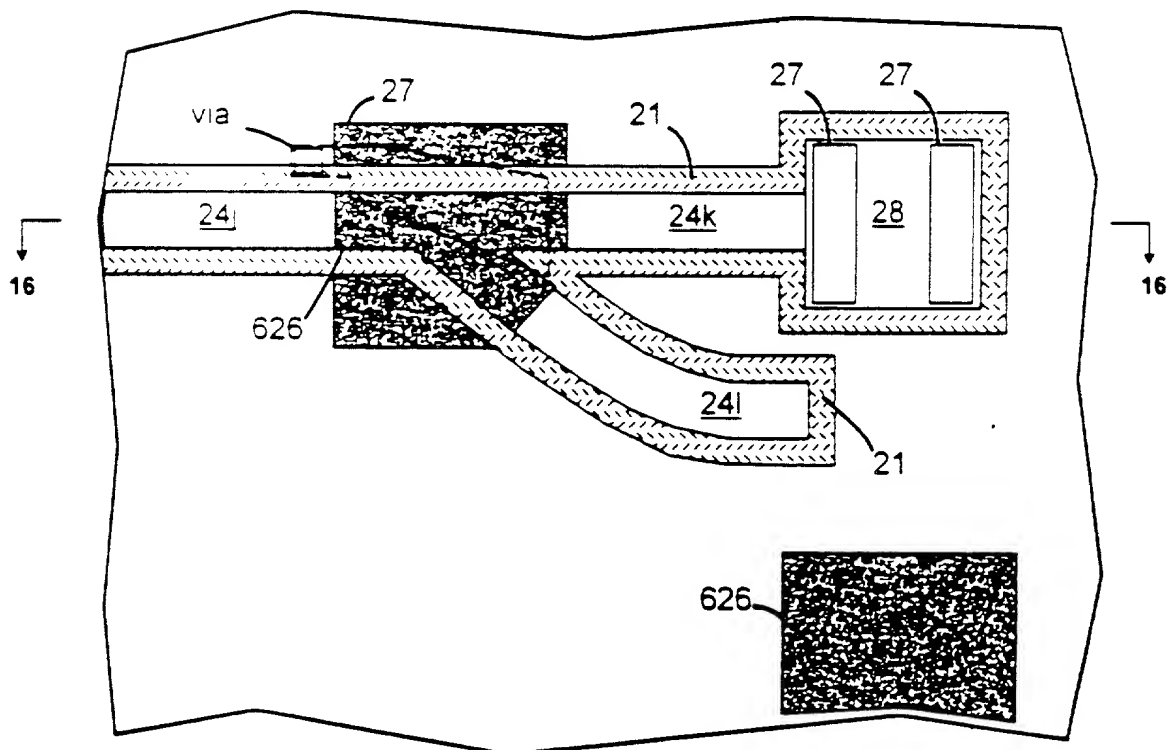


FIG. 20

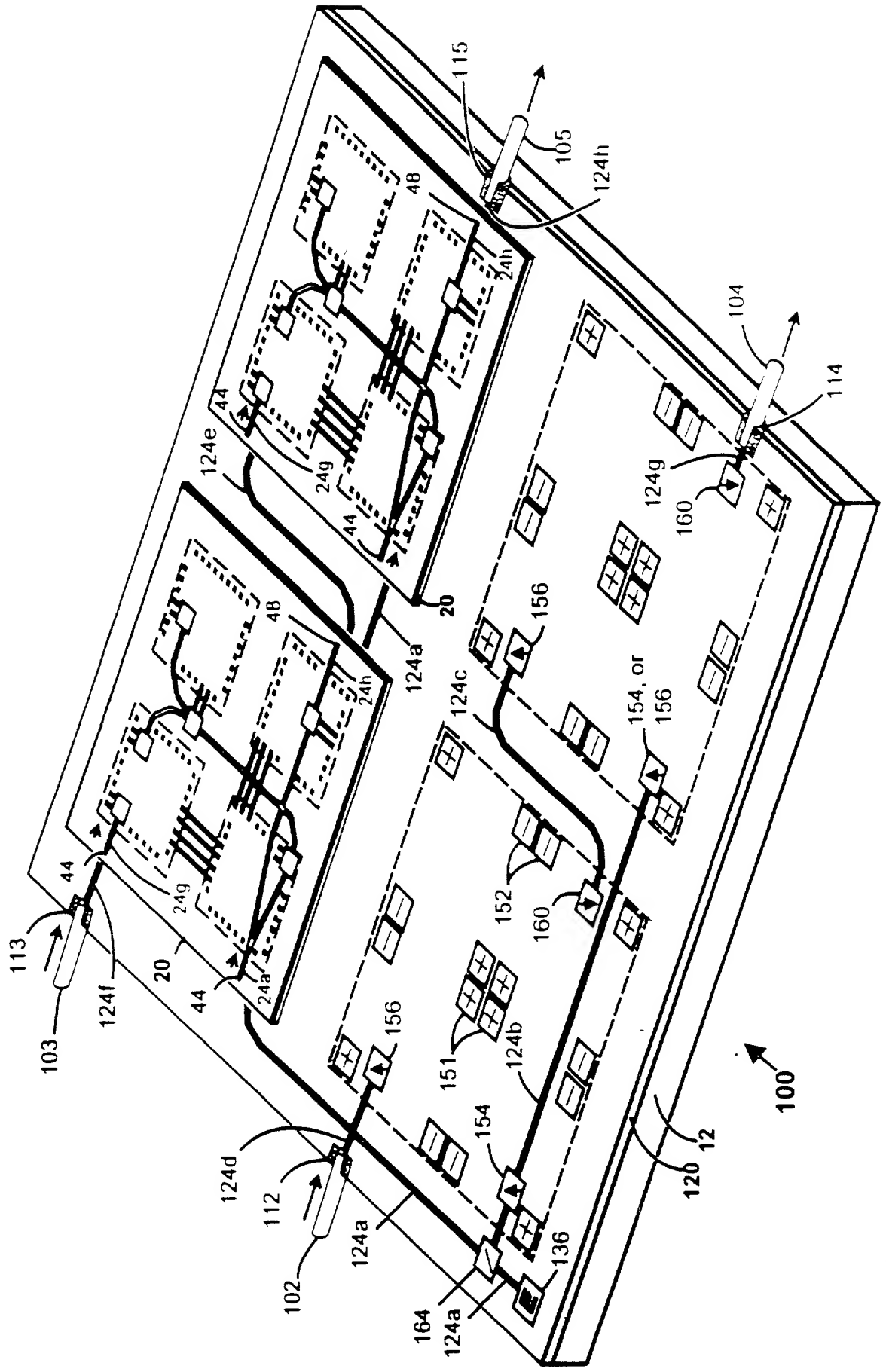


FIG. 21



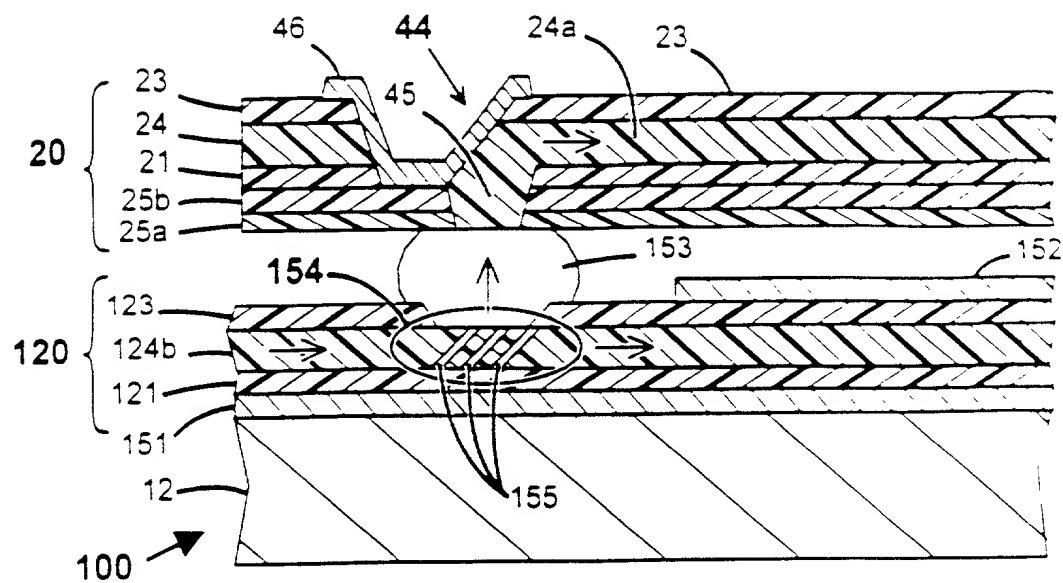


FIG. 22

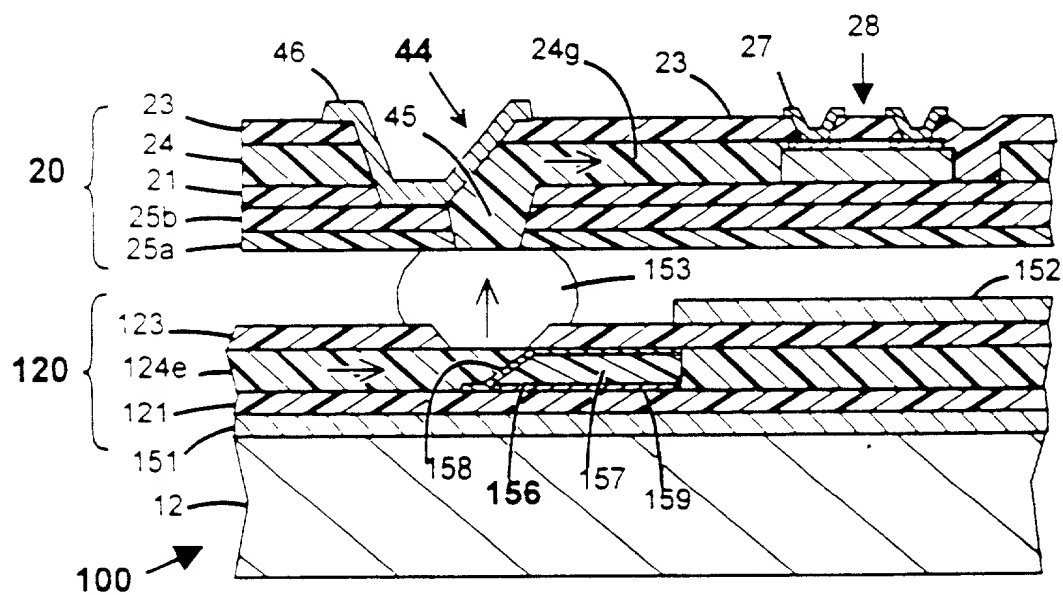


FIG. 23

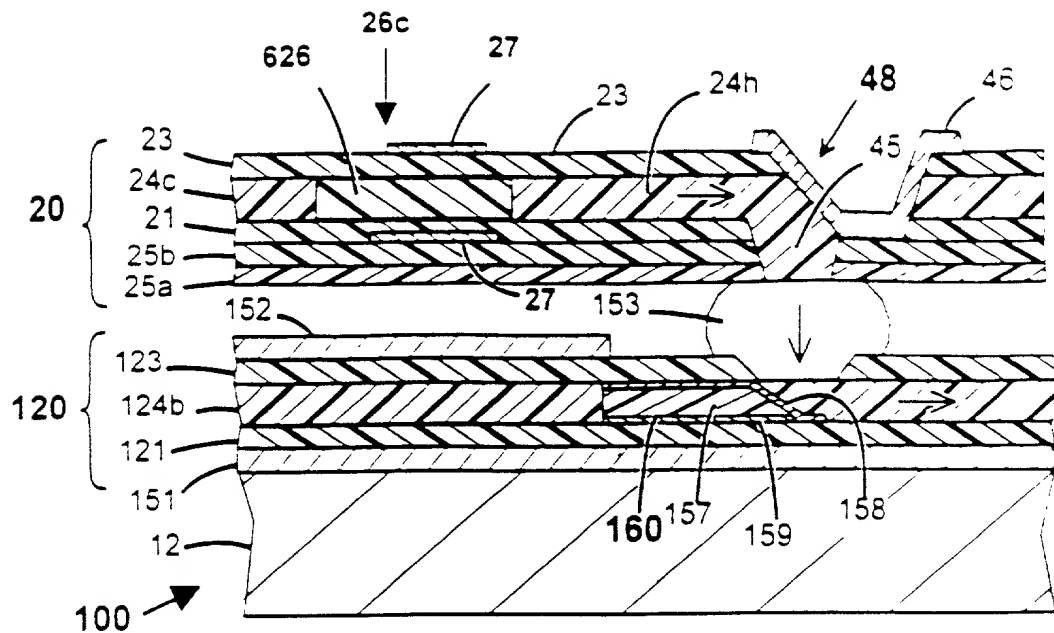


FIG. 24

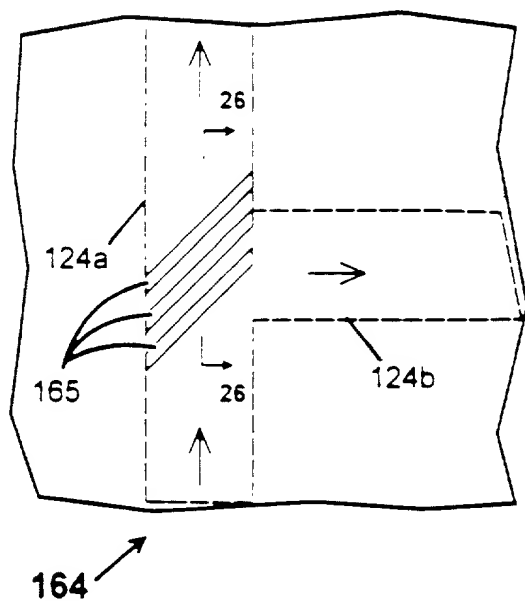


FIG. 25

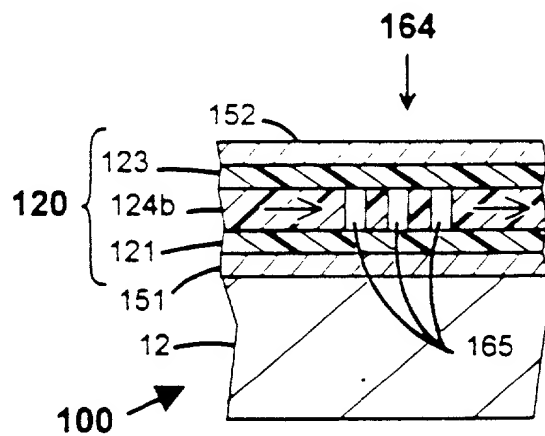


FIG. 26

FIG.\_27

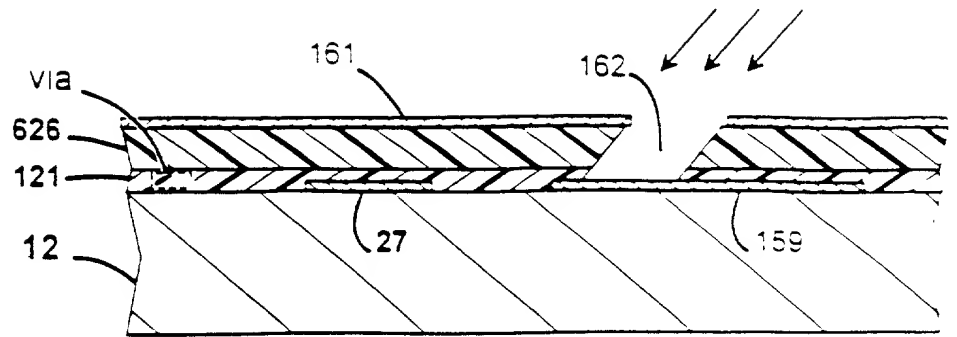


FIG.\_28

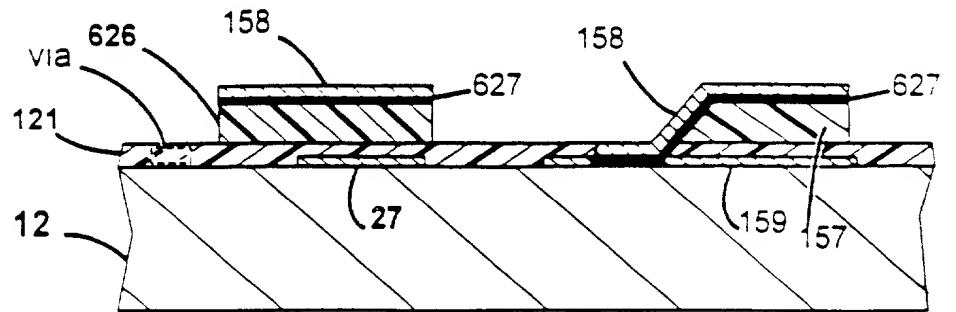


FIG.\_29

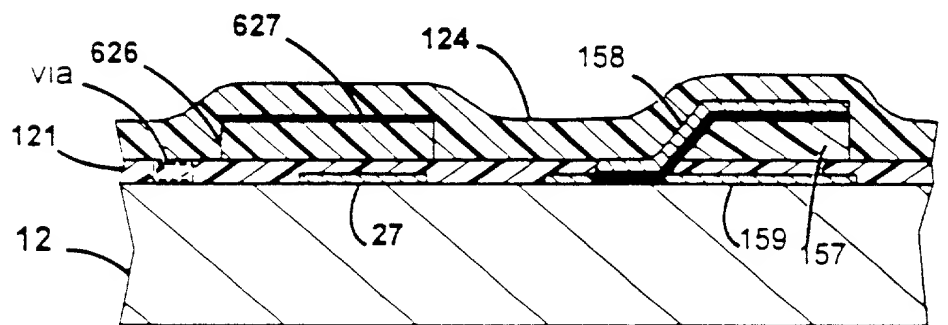
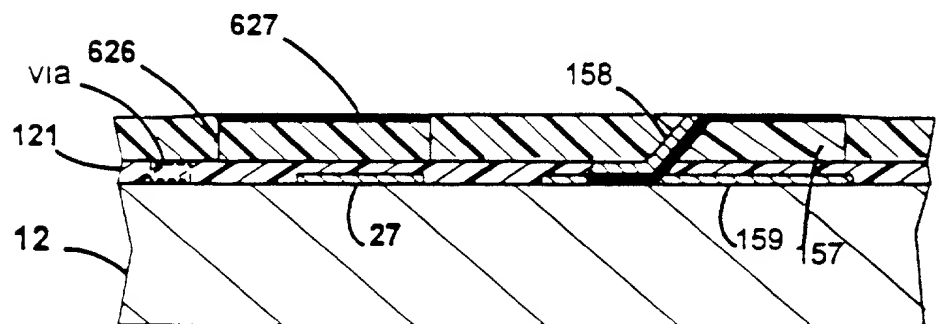
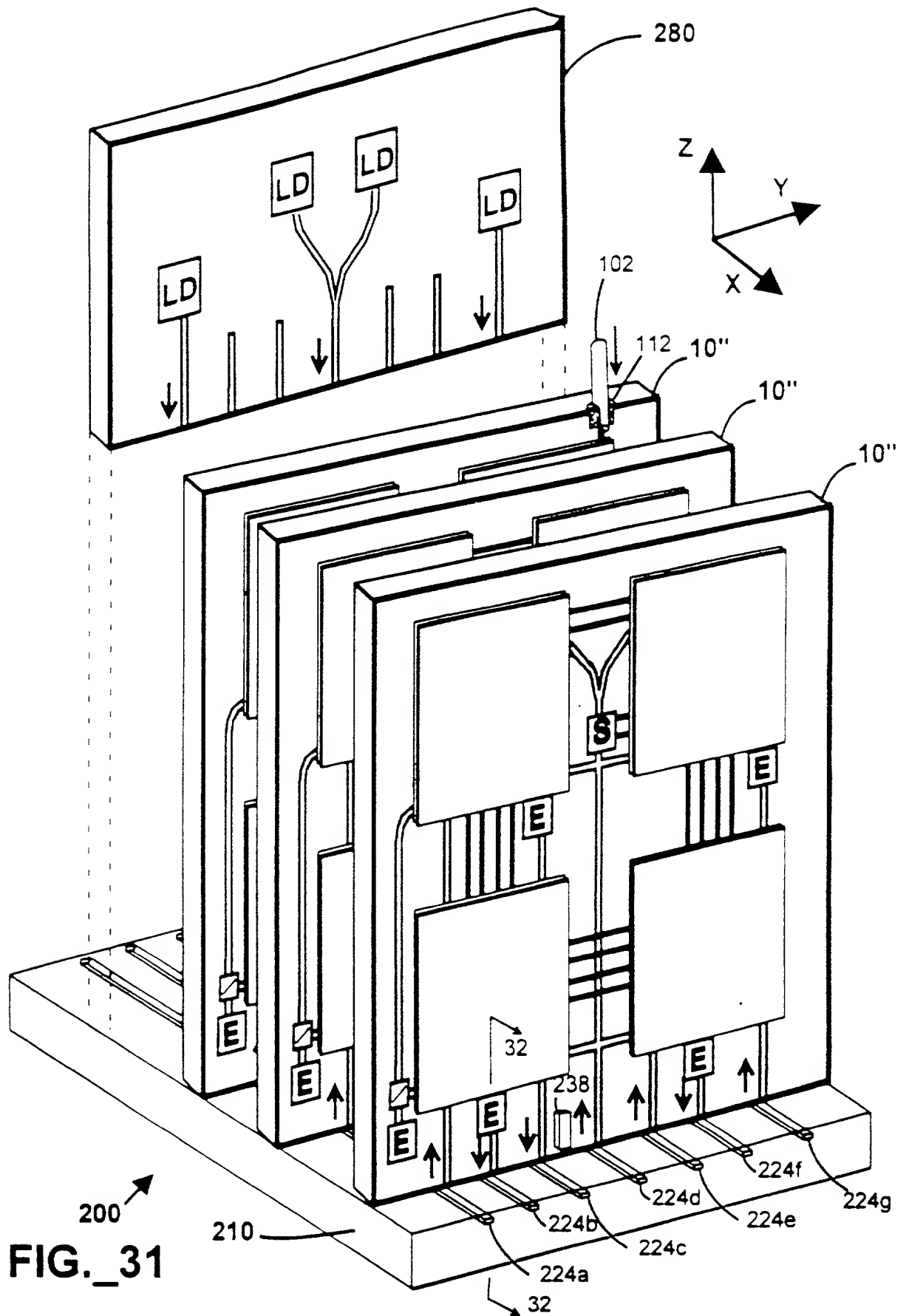
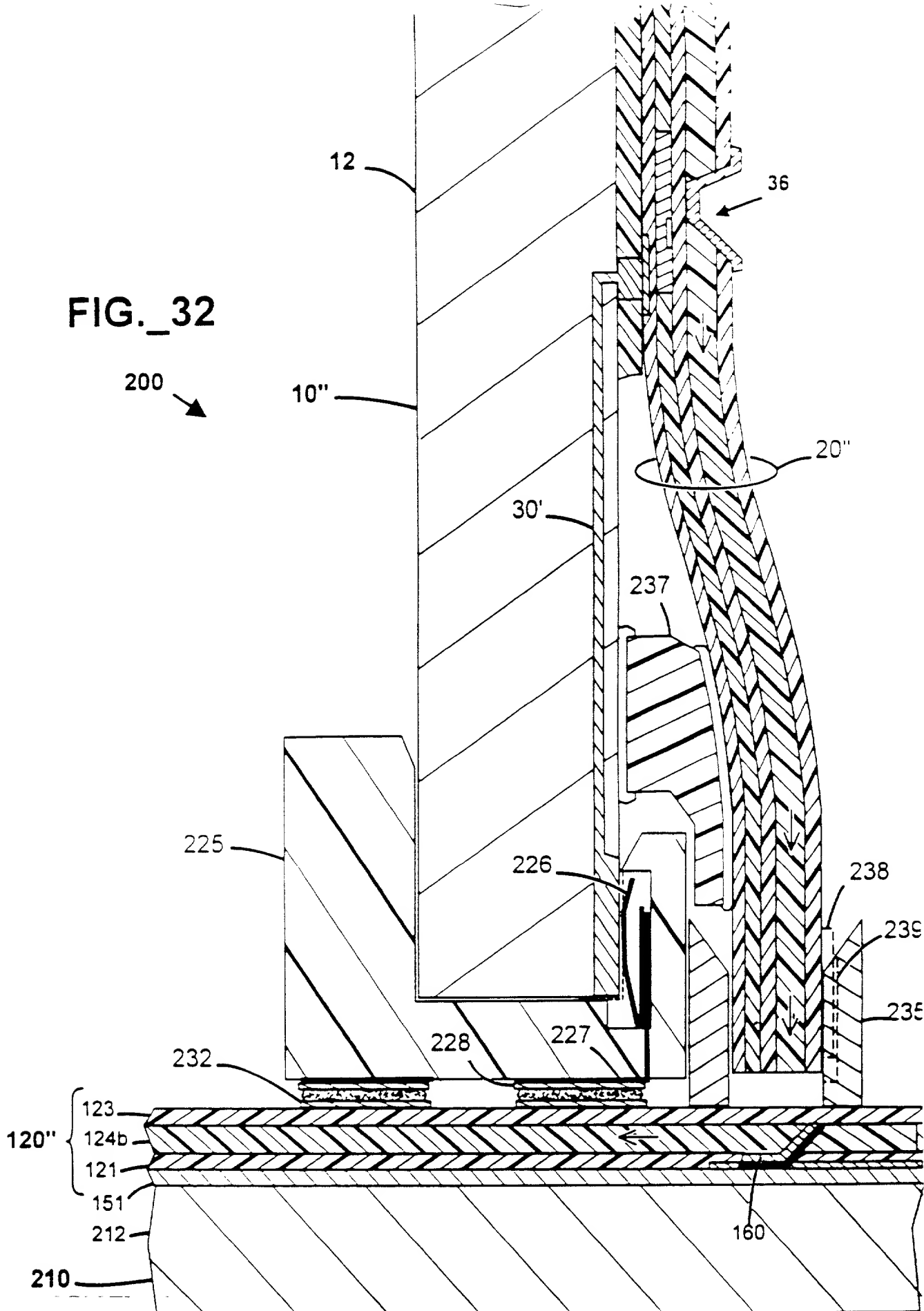
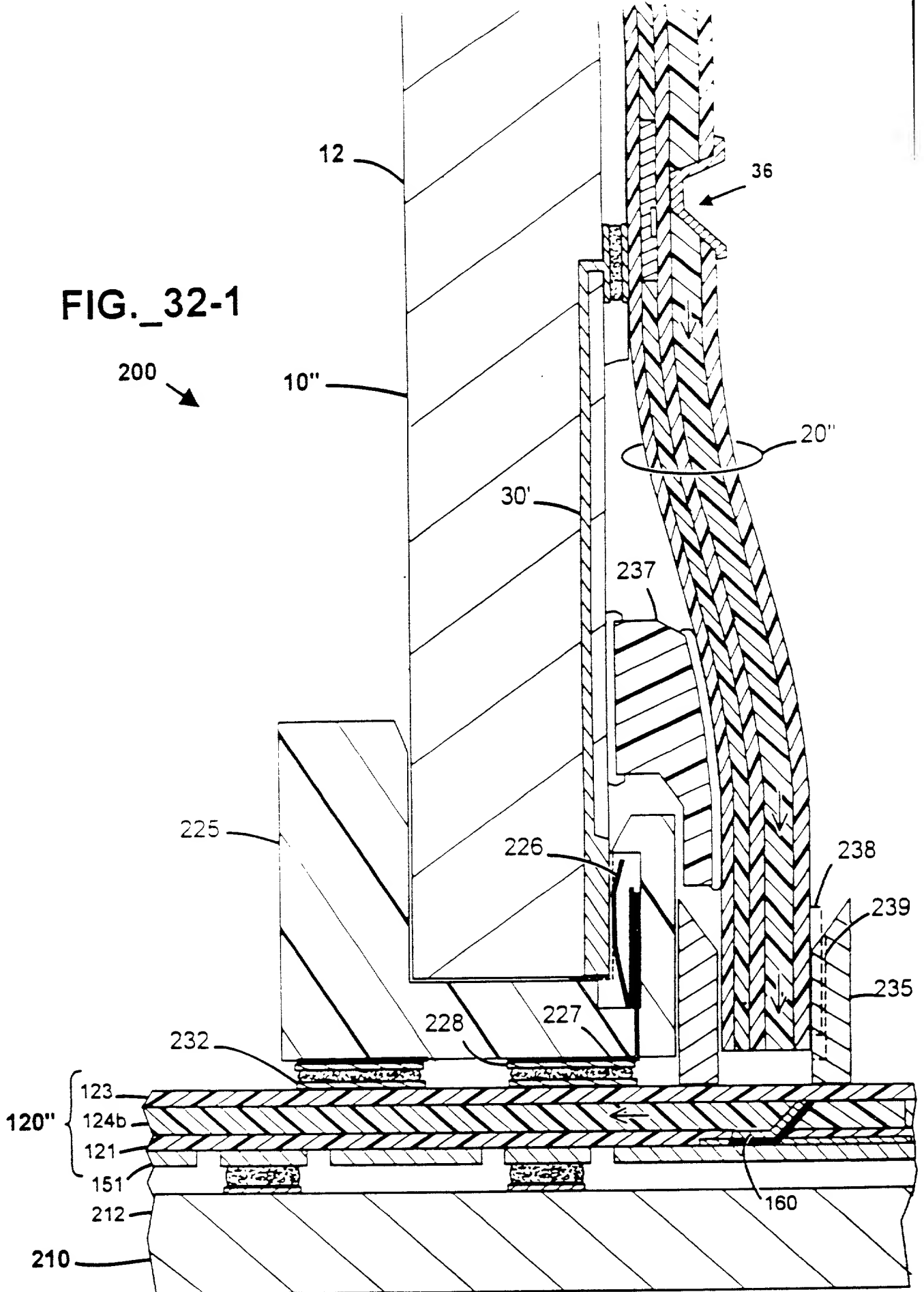


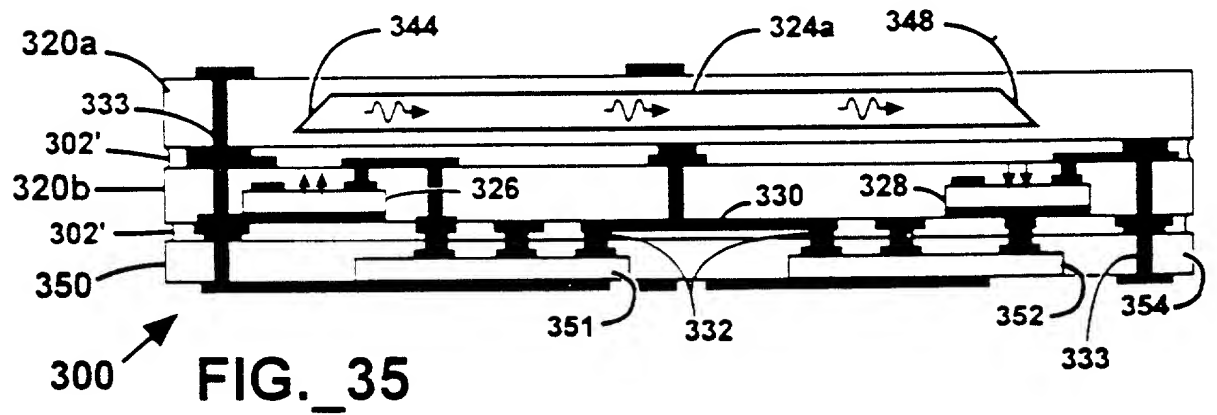
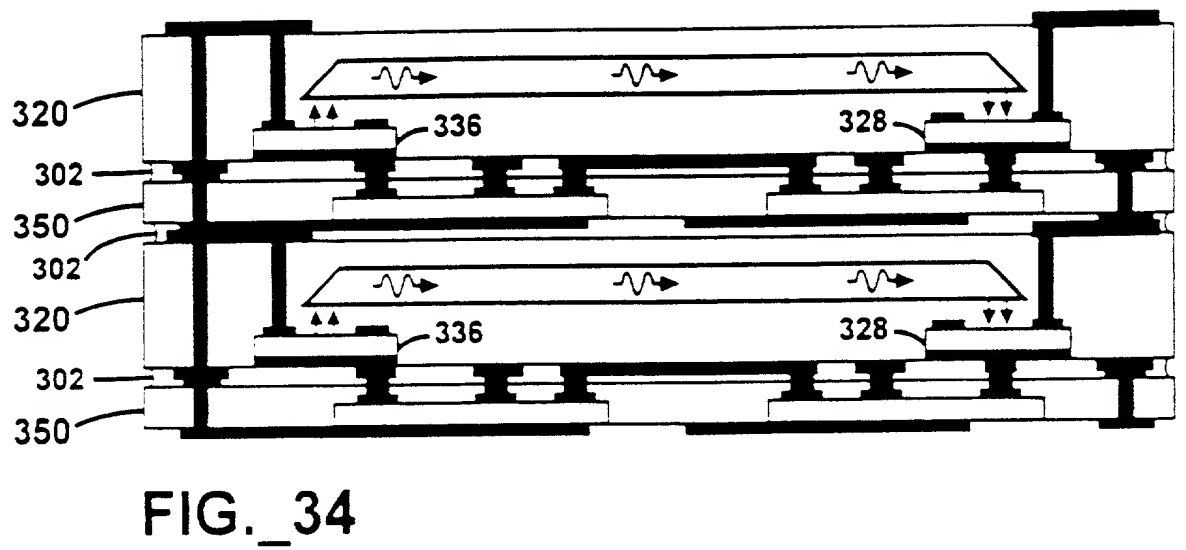
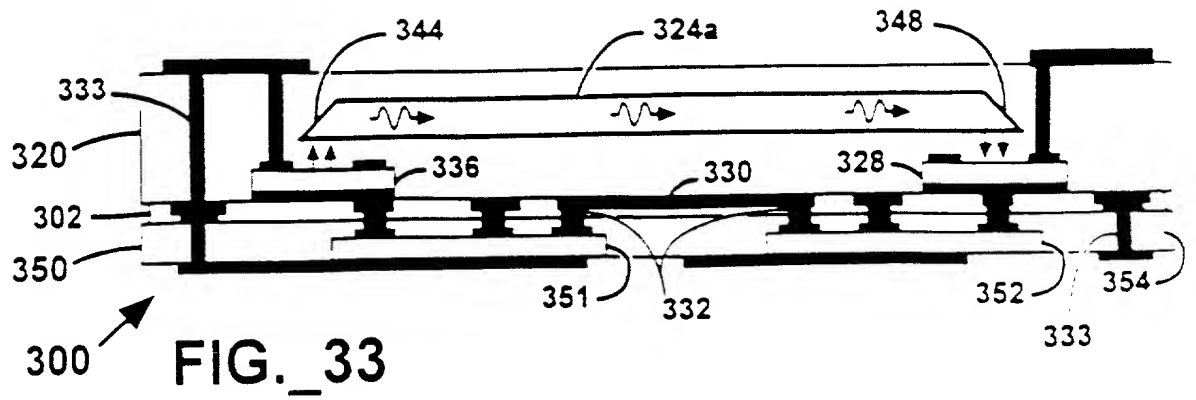
FIG.\_30











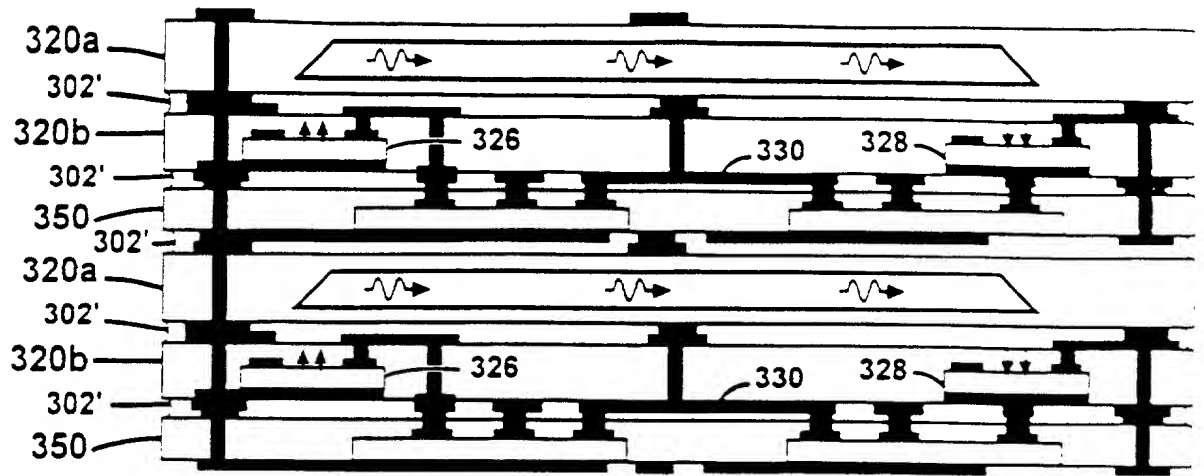


FIG. 36

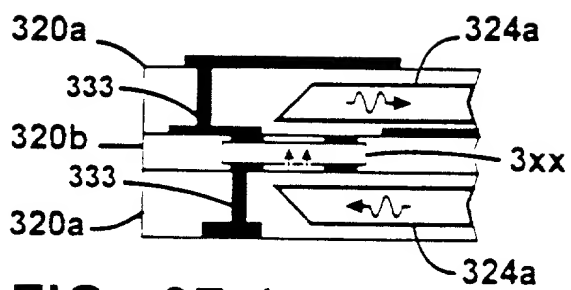


FIG. 37-1

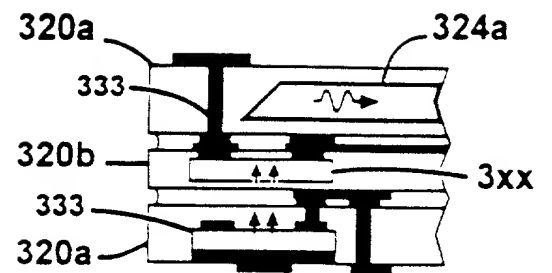


FIG. 37-2

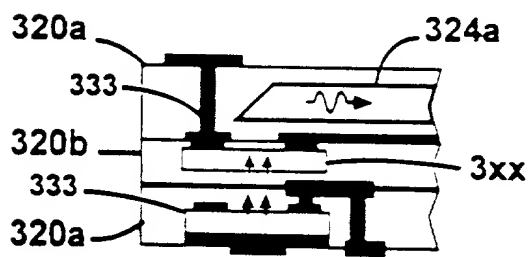


FIG. 37-3

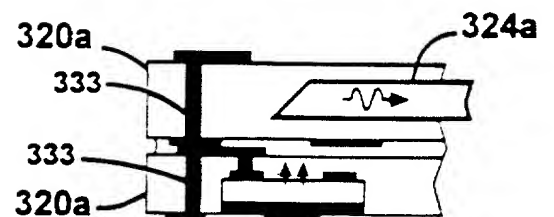


FIG. 37-4



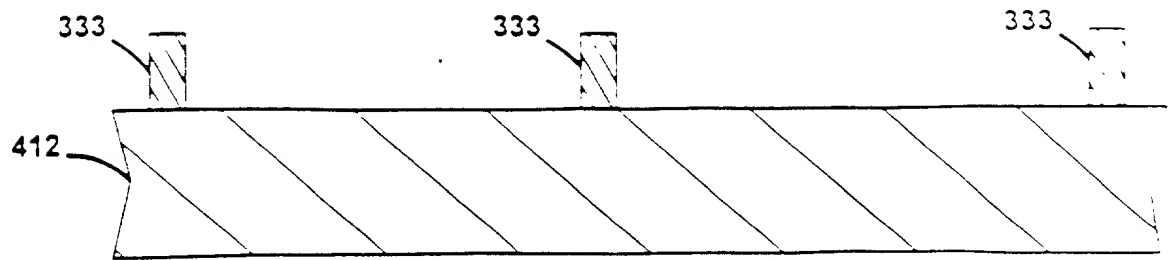


FIG. 38

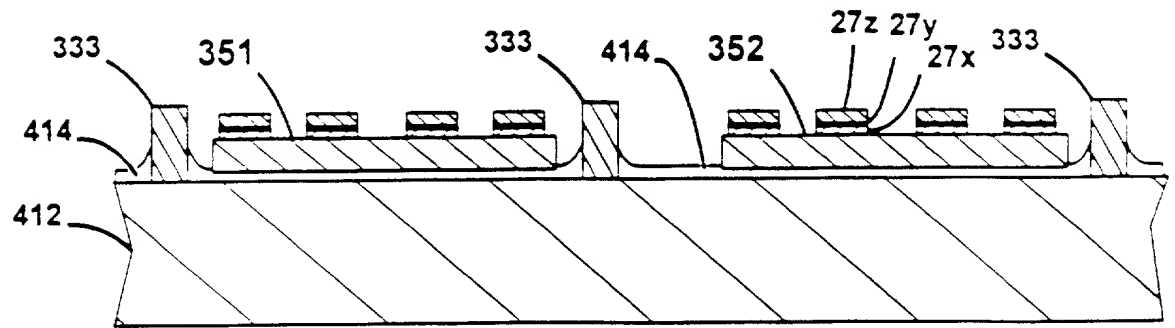


FIG. 39

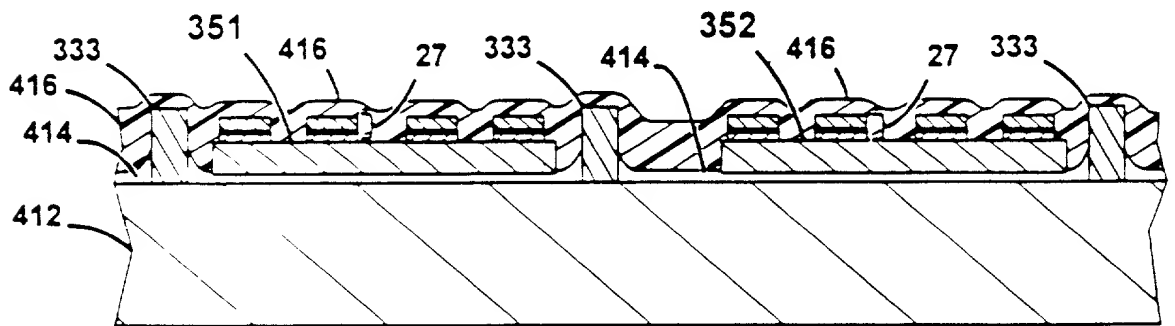


FIG. 40

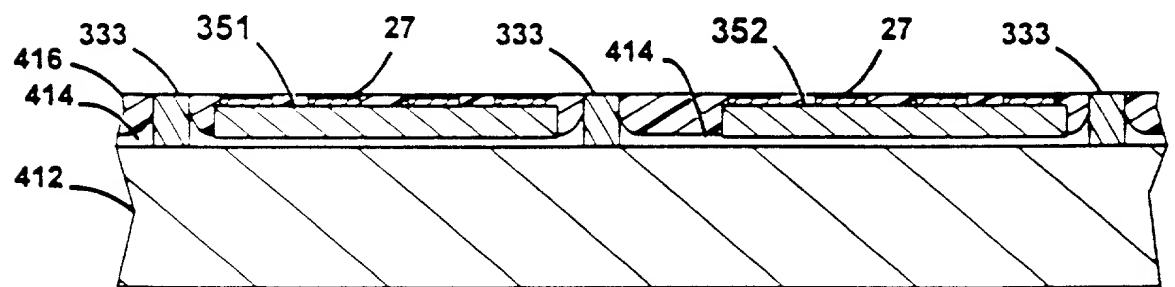


FIG. 41

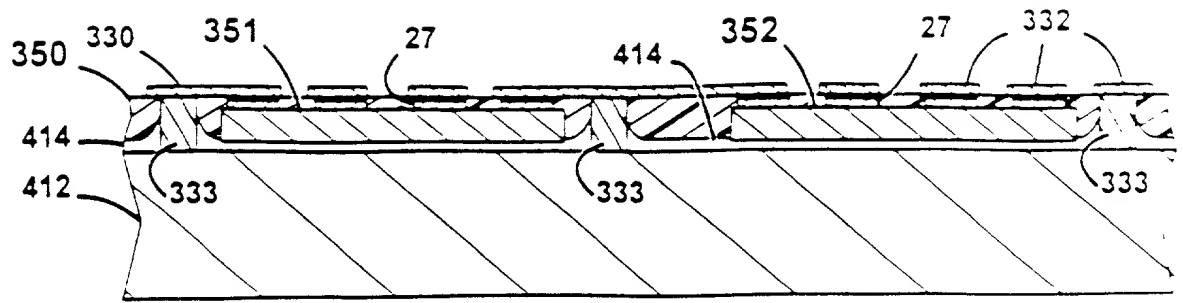


FIG. 42

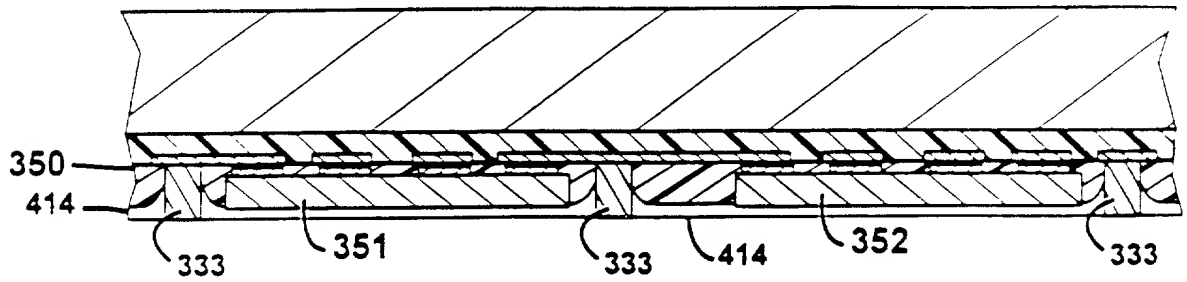


FIG. 43

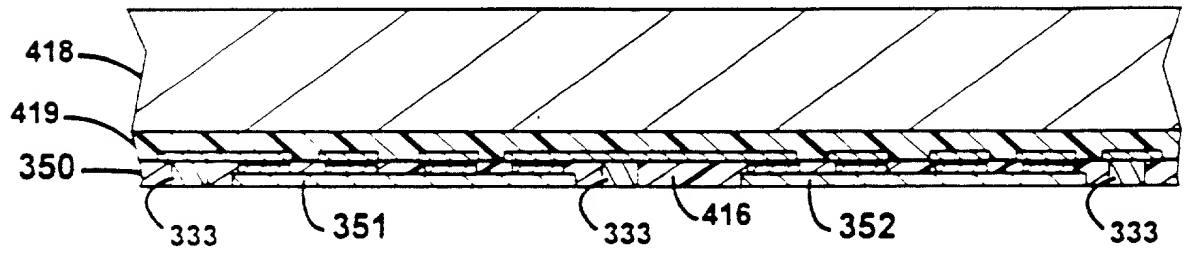


FIG. 44

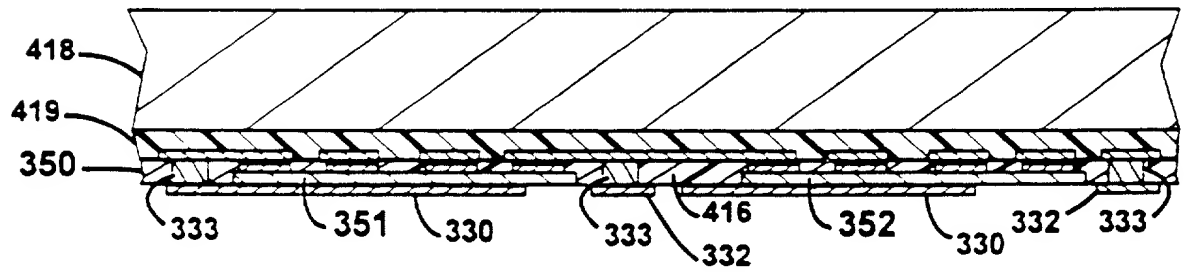
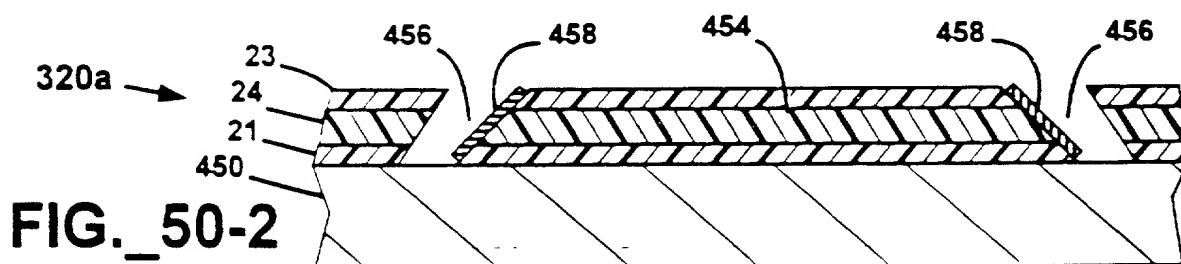
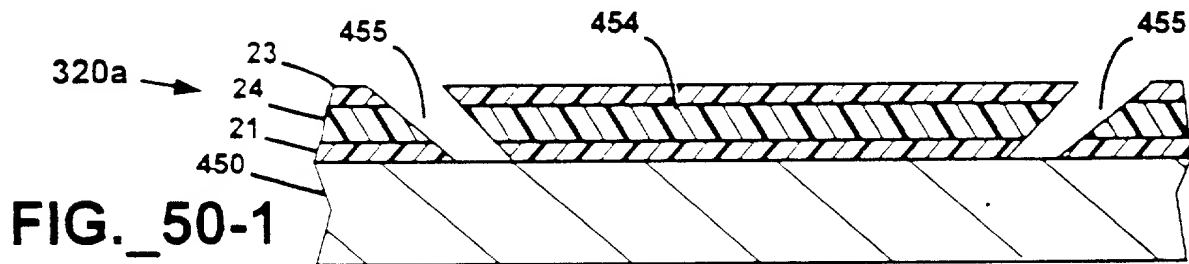
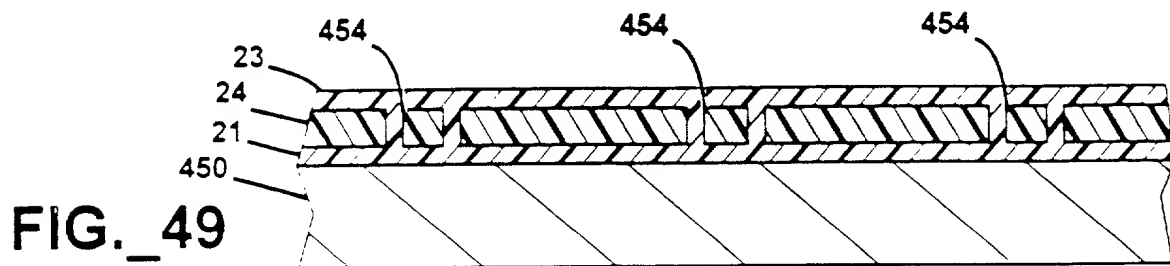
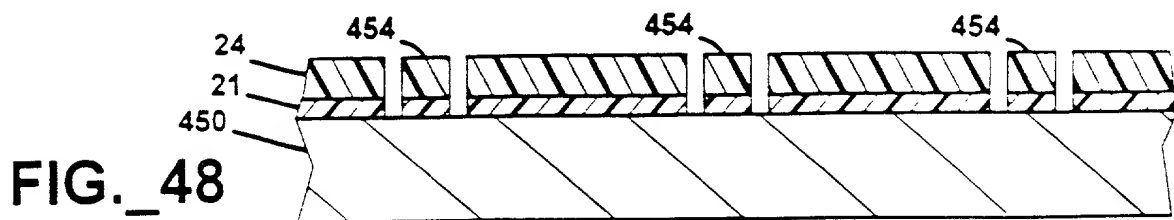
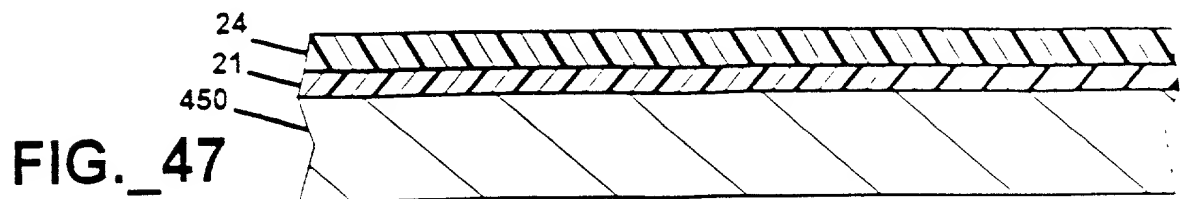
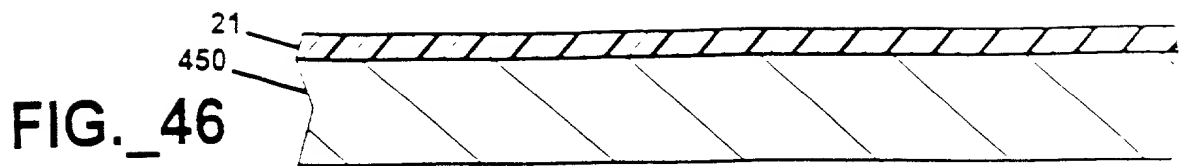
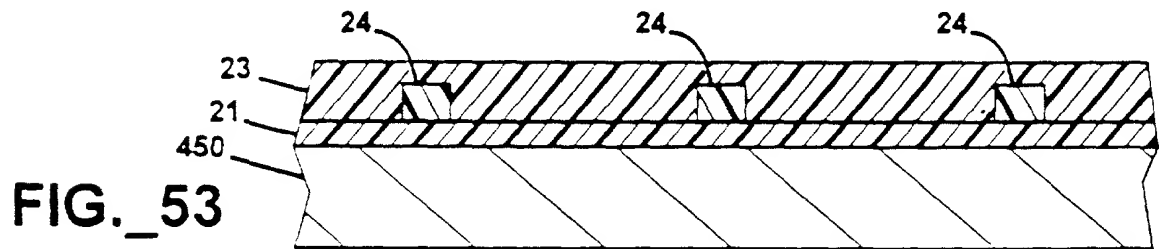
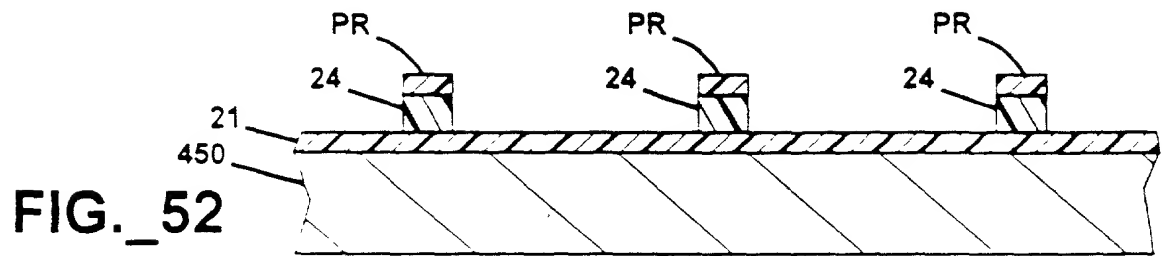
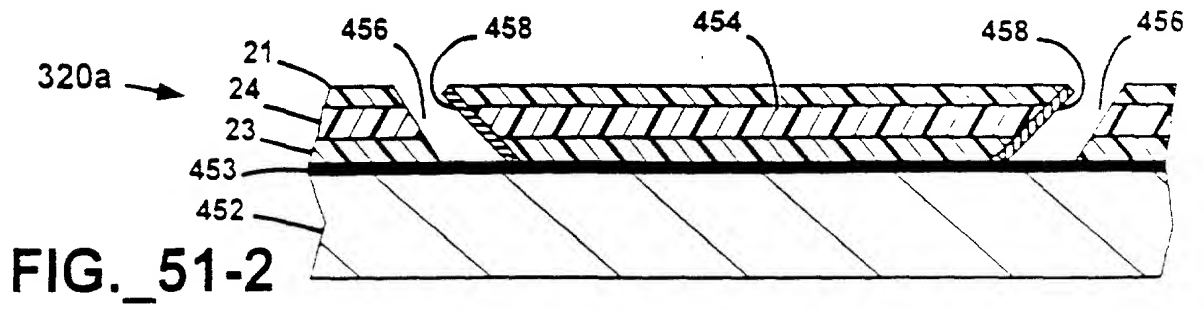
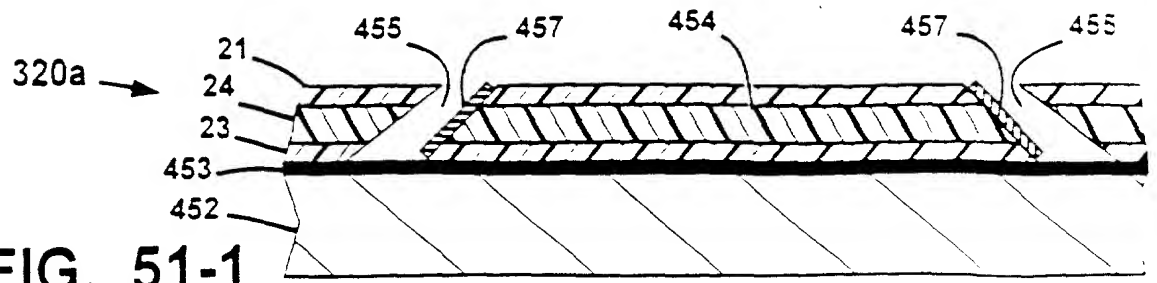
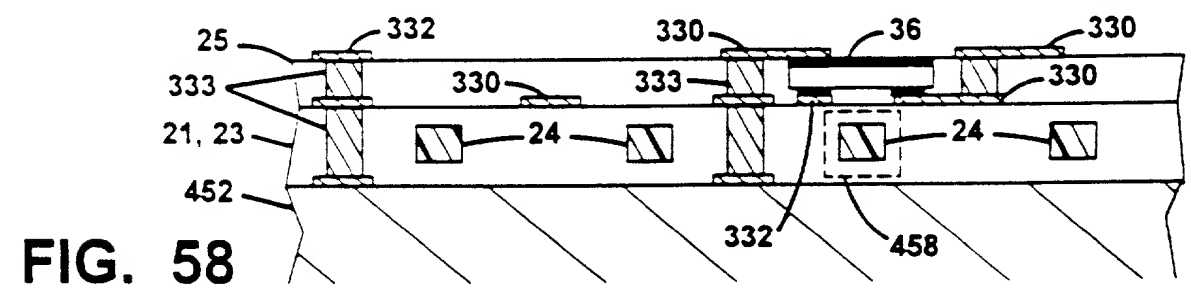
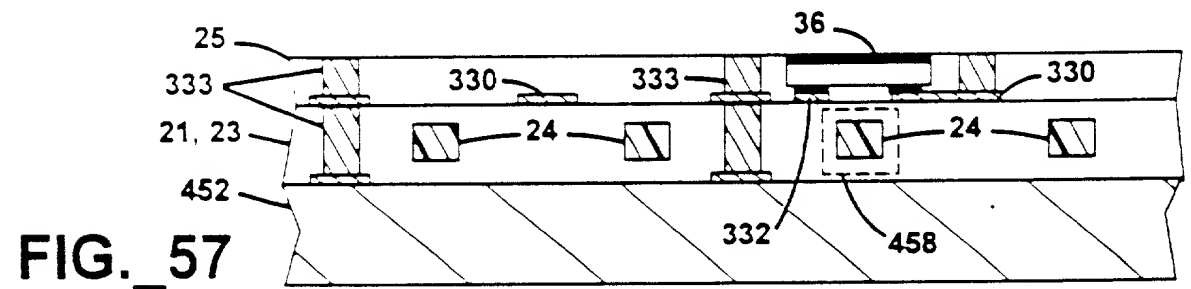
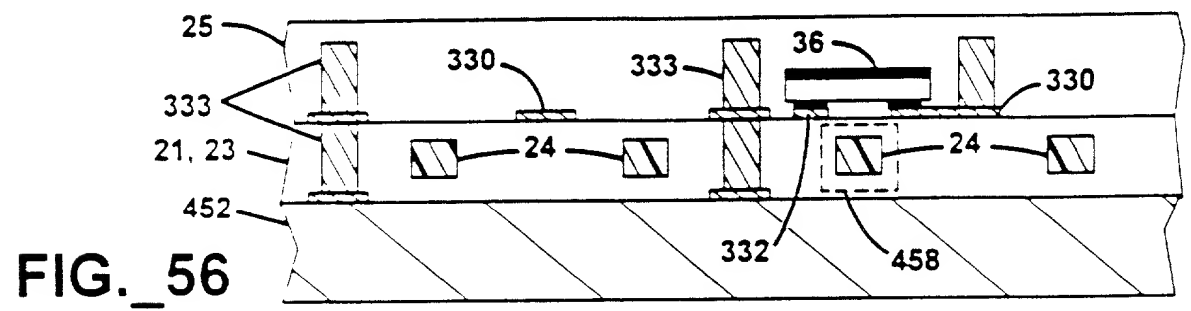
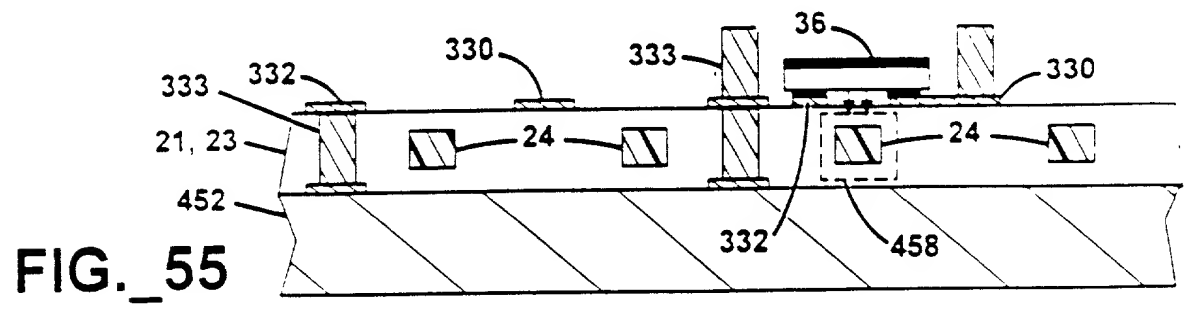
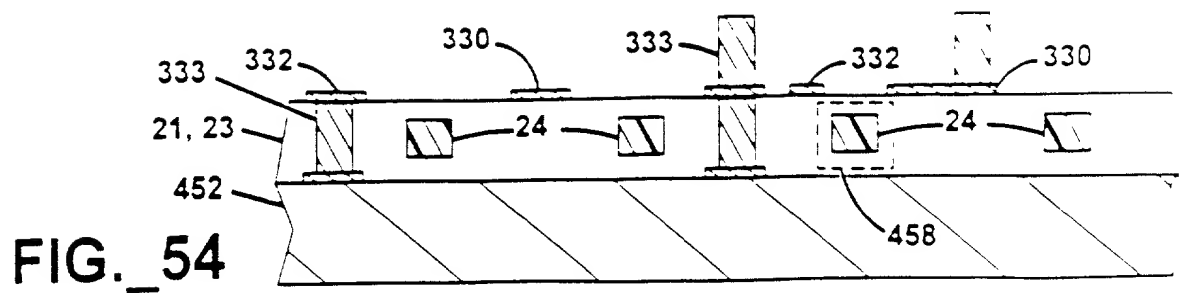


FIG. 45







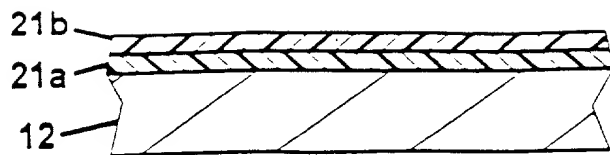


FIG.\_59

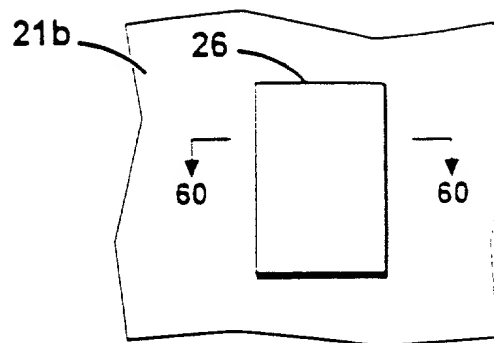


FIG.\_61

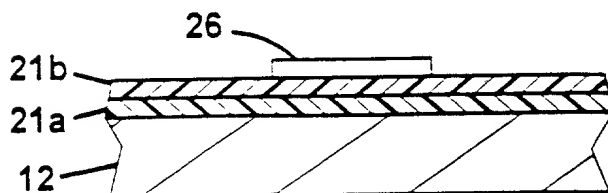


FIG.\_60

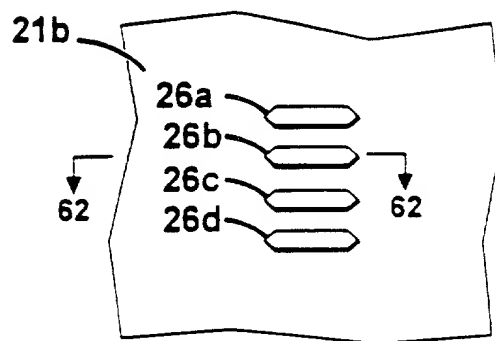


FIG.\_63

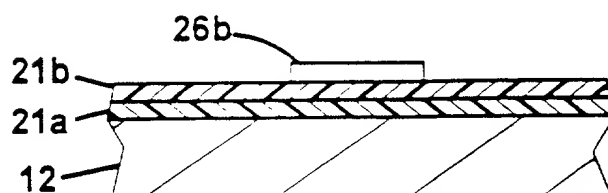


FIG.\_62

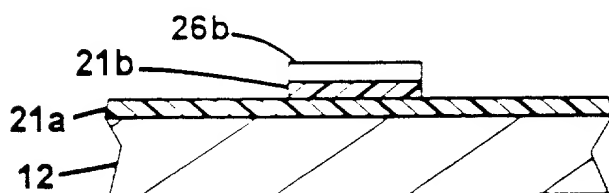


FIG.\_64

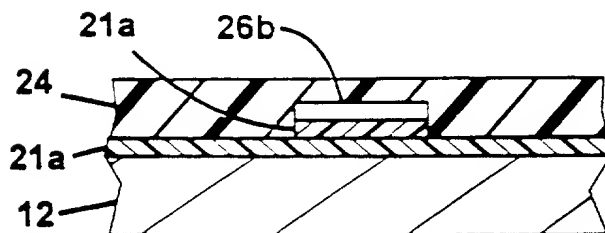
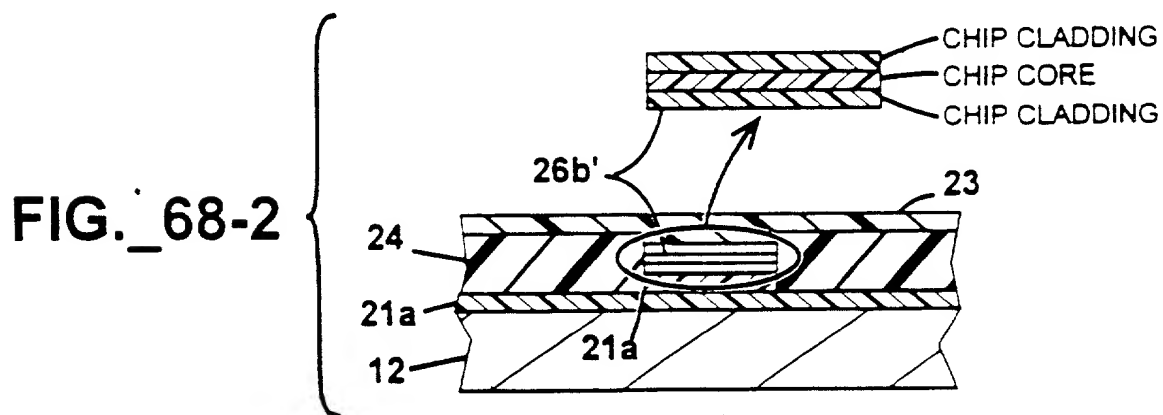


FIG.\_65



09767582.012201

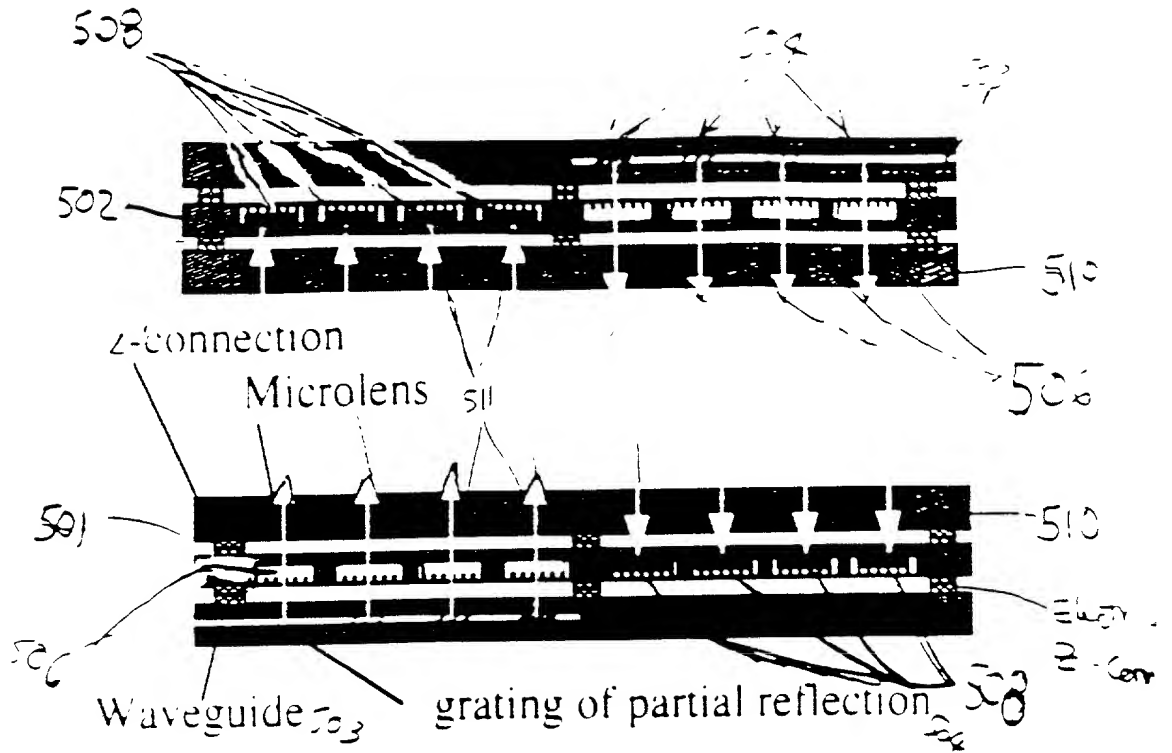


FIG. 69

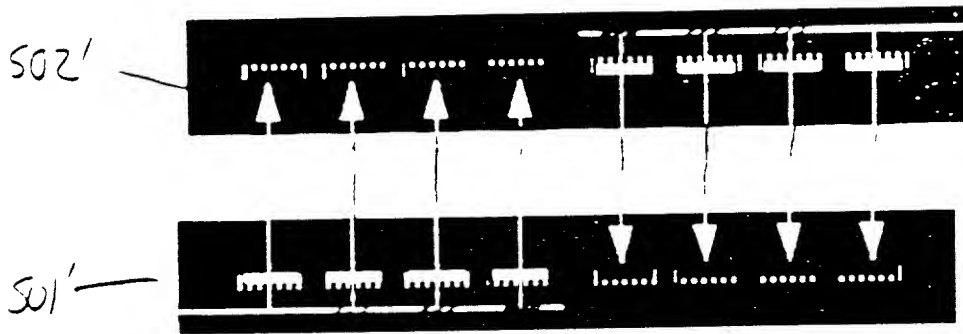
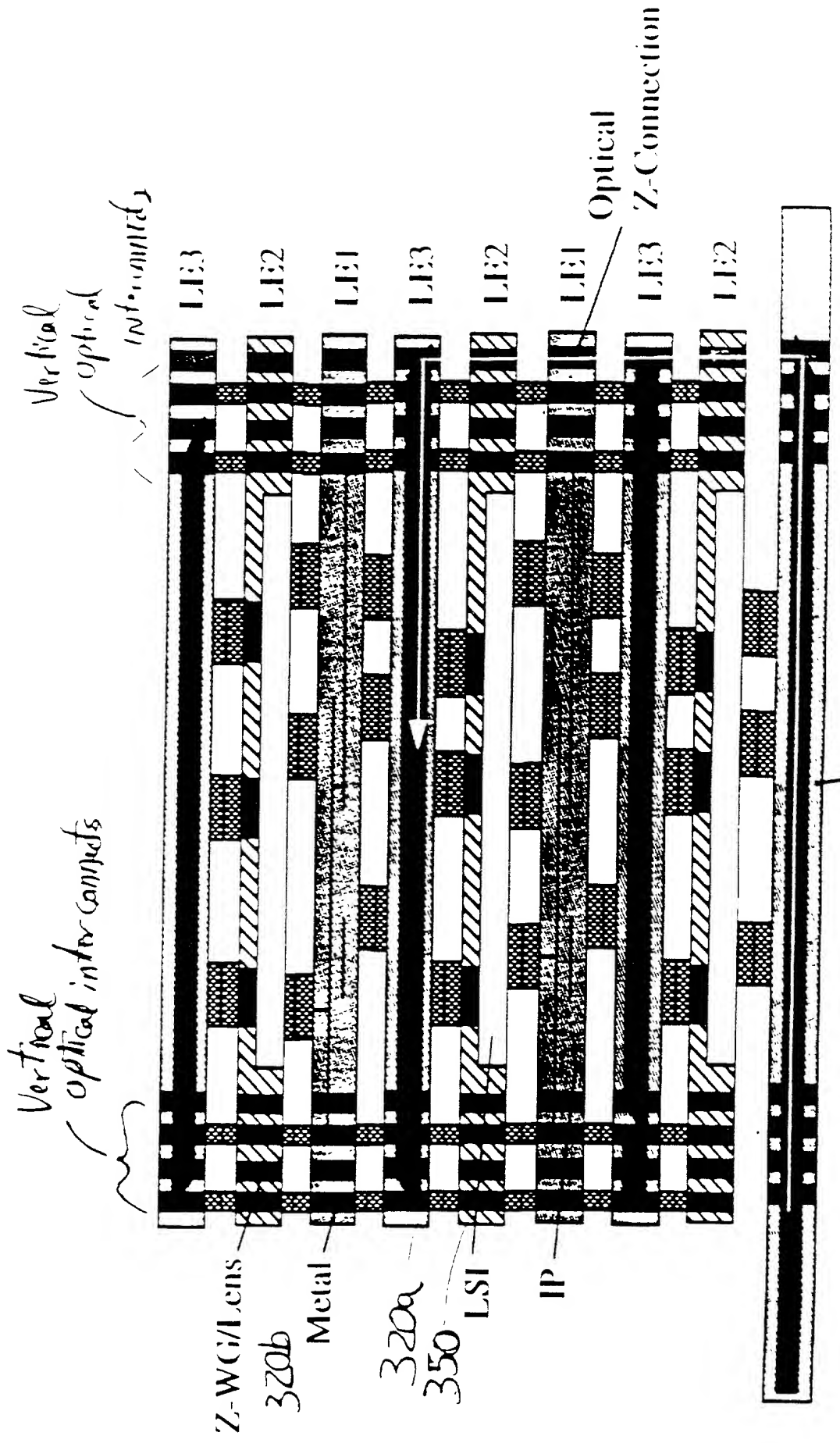


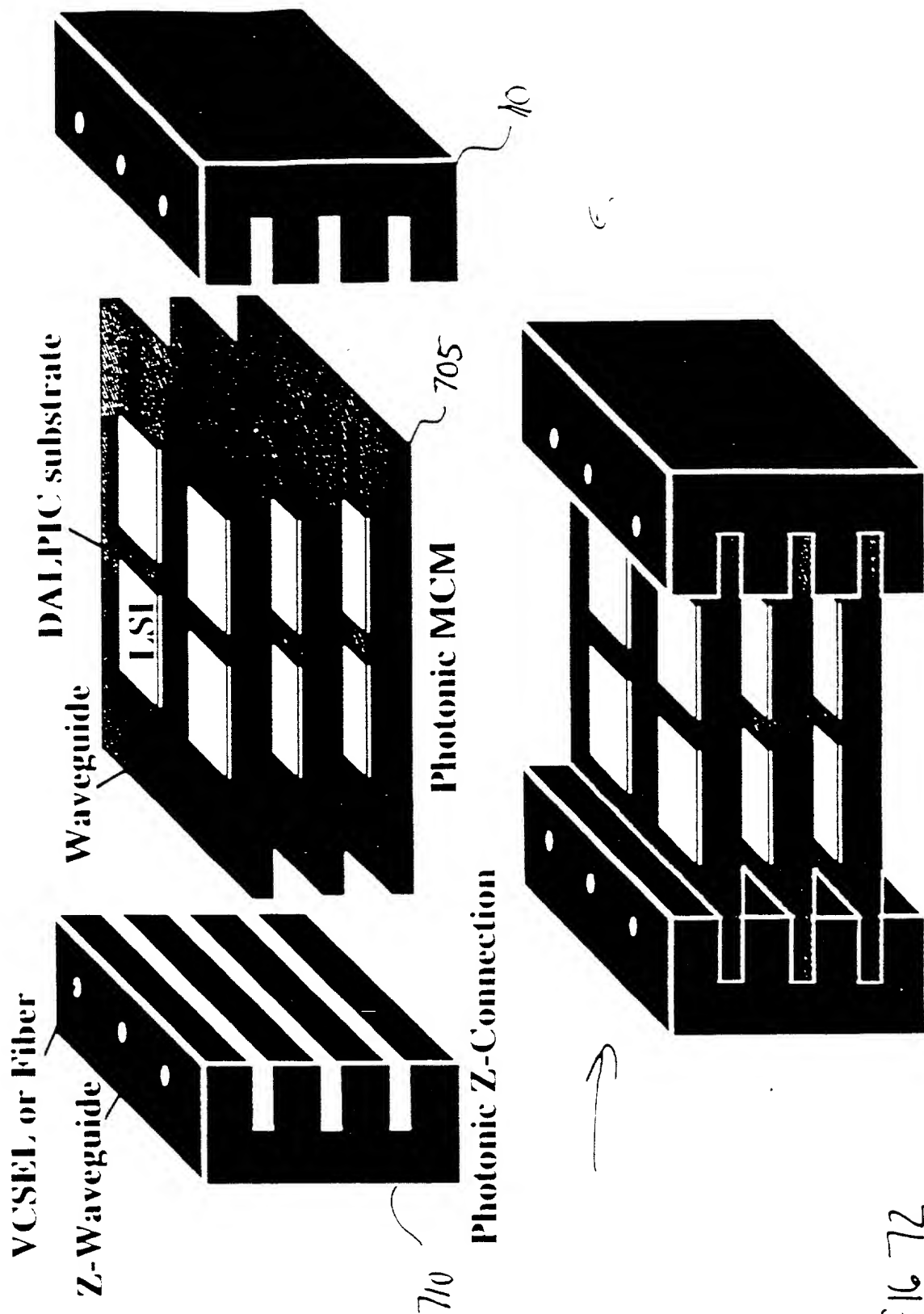
FIG. 70



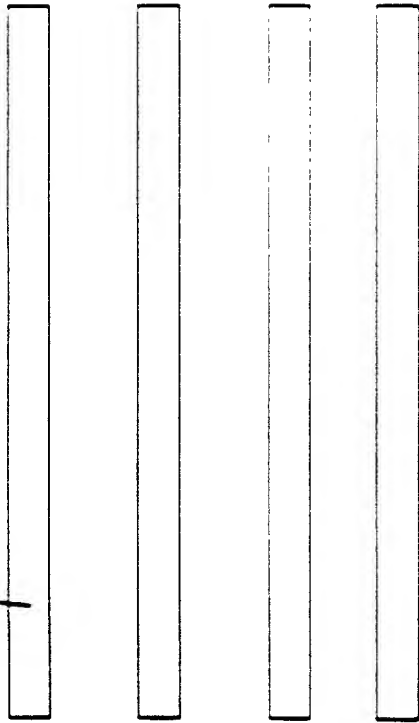


Optical Backplane

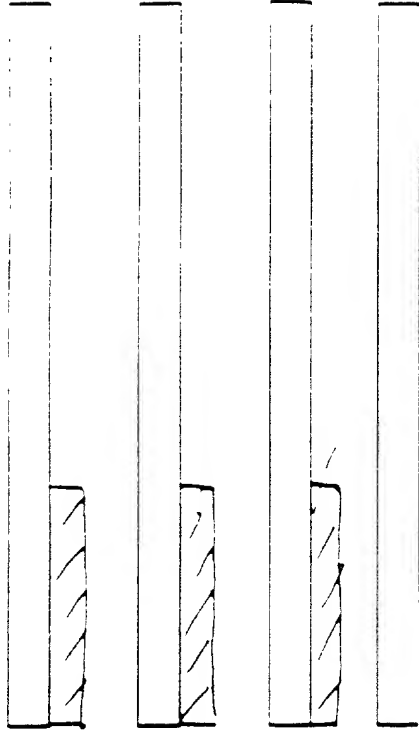
FIG. 71



Flexible Photo-imagable sheet (Polyguide)

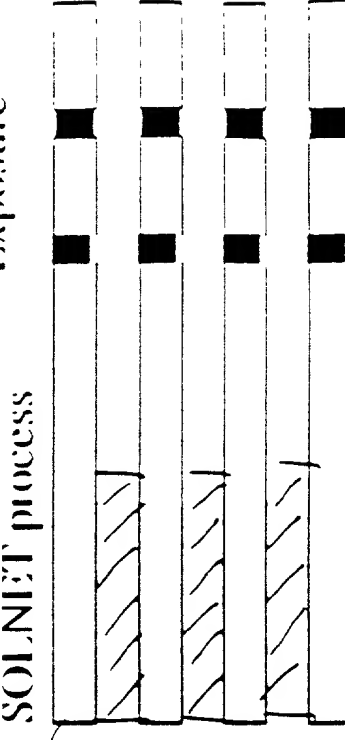
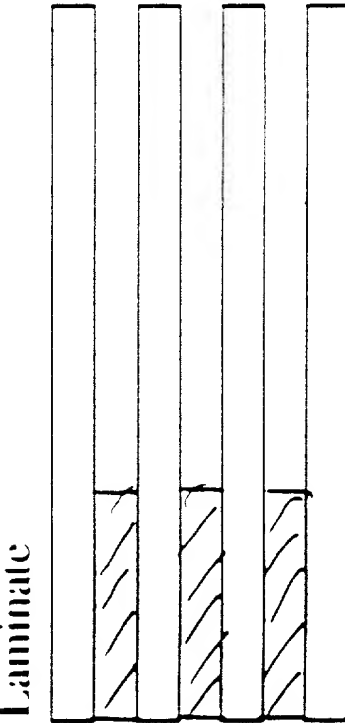


Bonding sheet attach

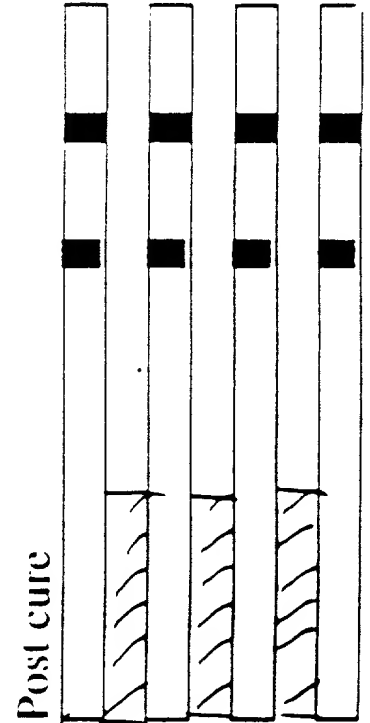


SOLNET process

Exposure



Post cure



Assemble

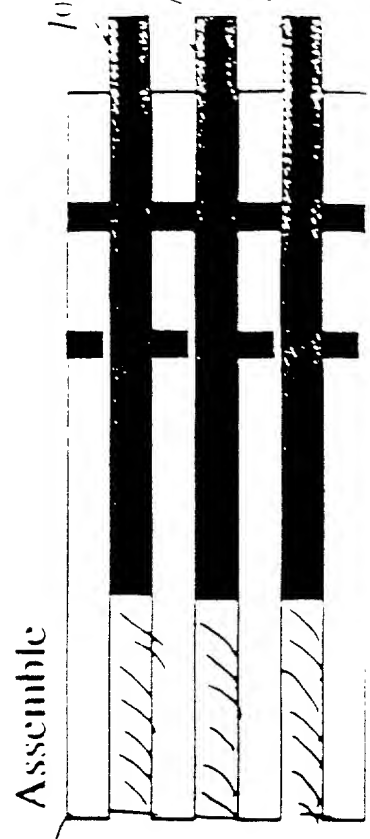
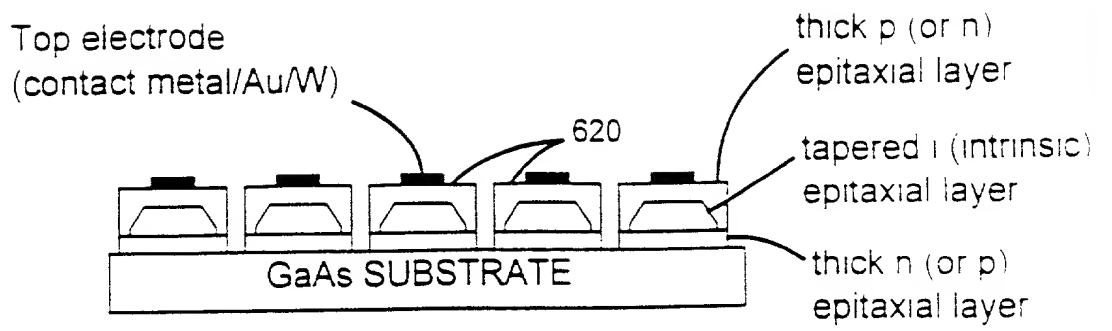
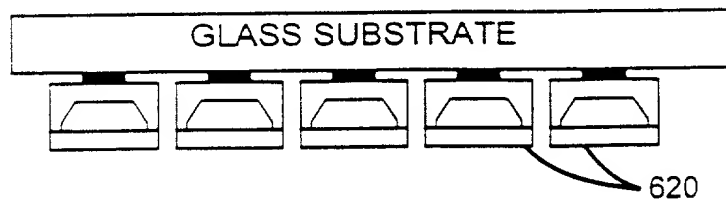


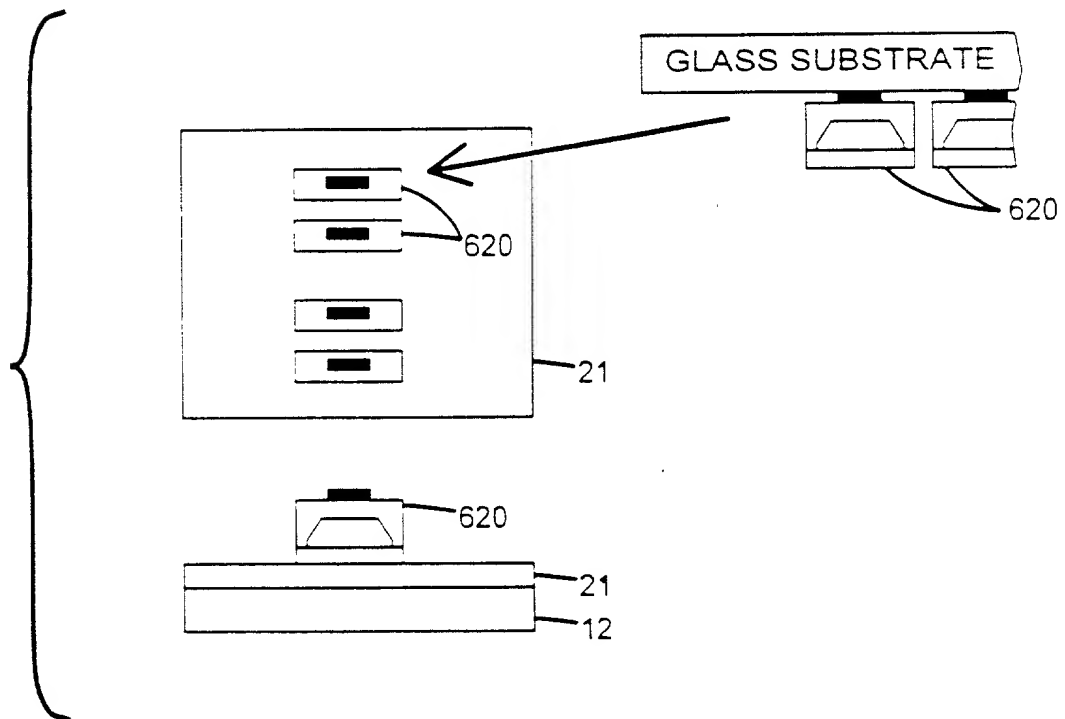
FIG. 10



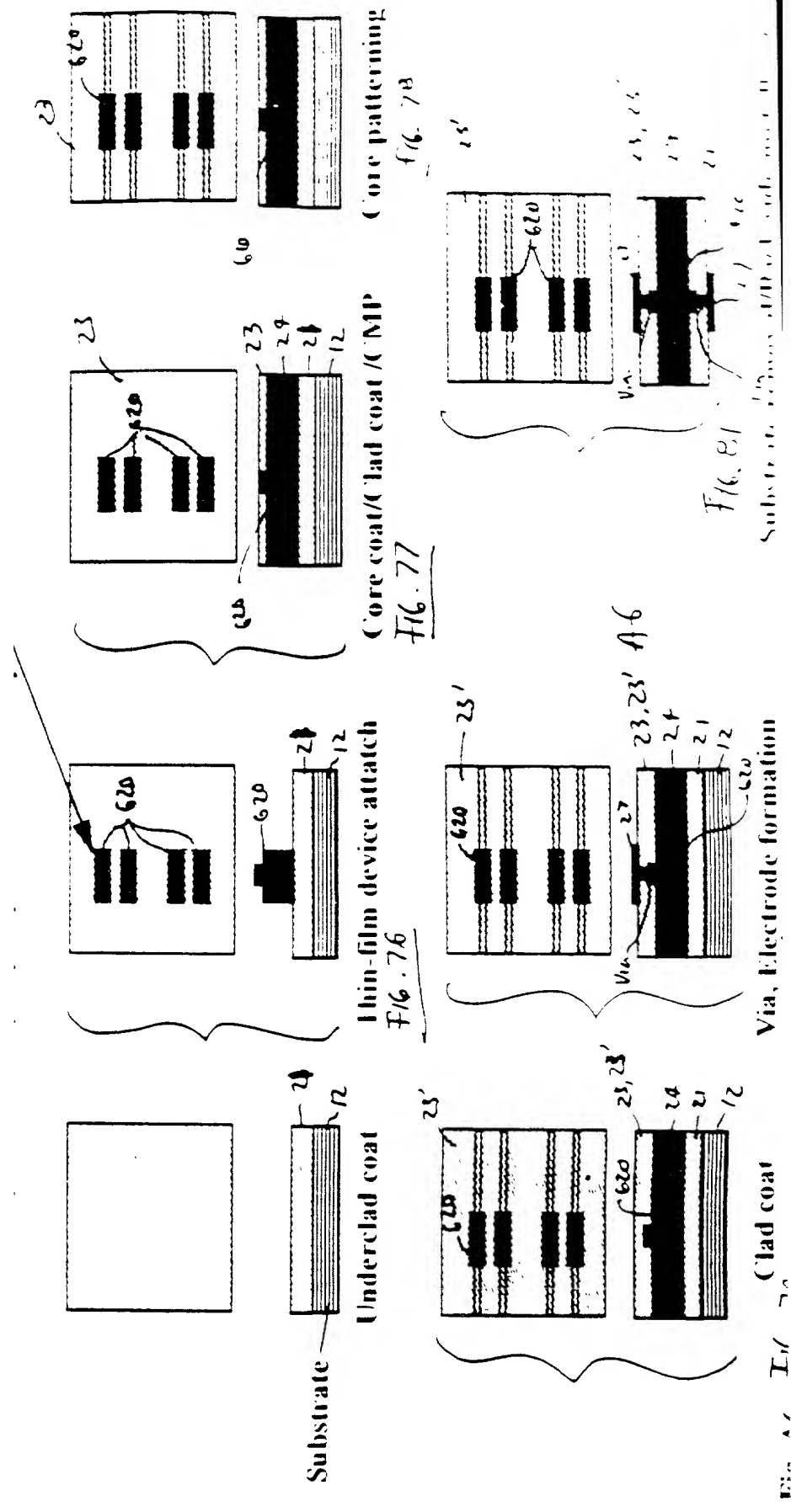
**FIG.\_74** (Epitaxial growth and patterning)



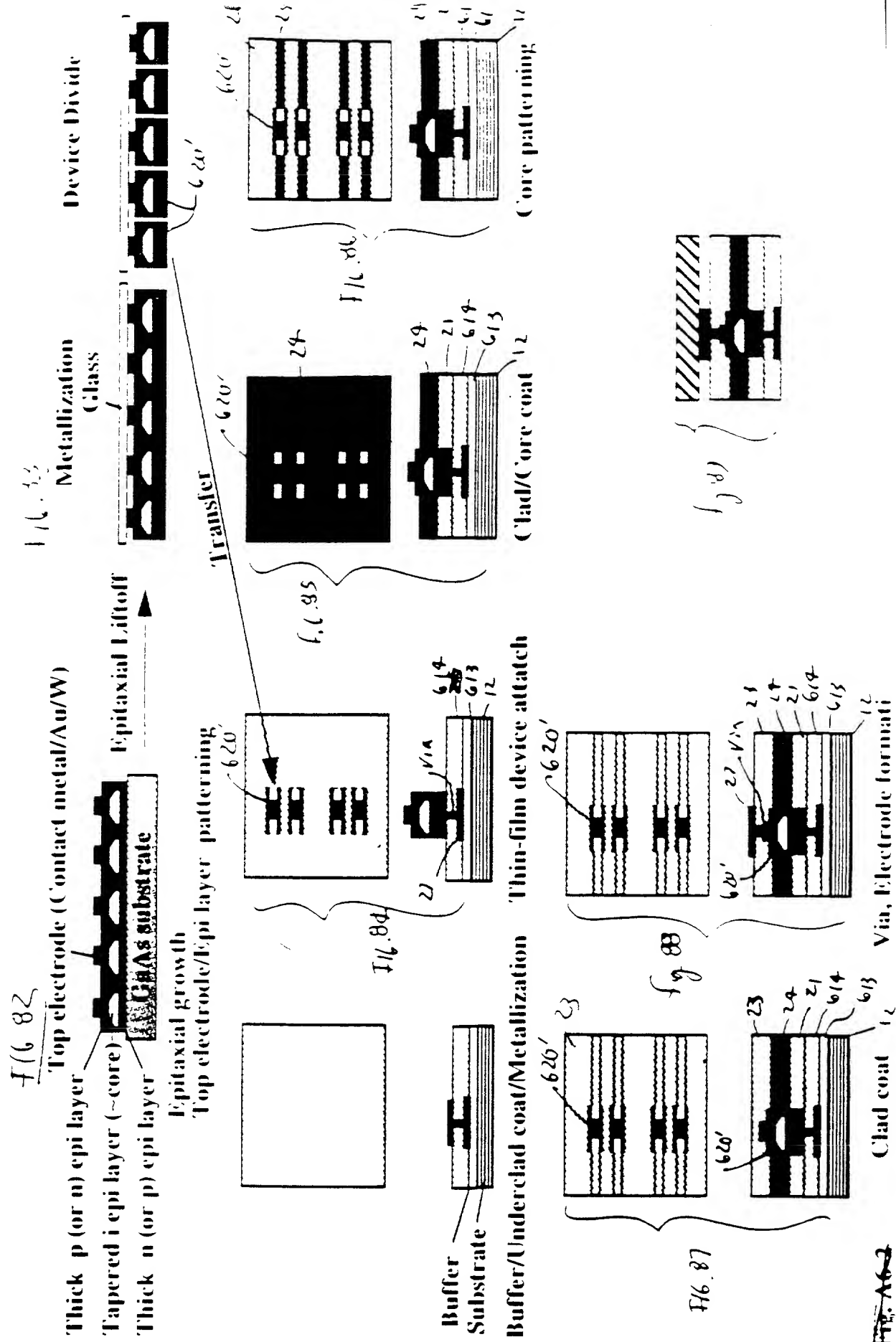
**FIG.\_75** (Epitaxial lift-off)

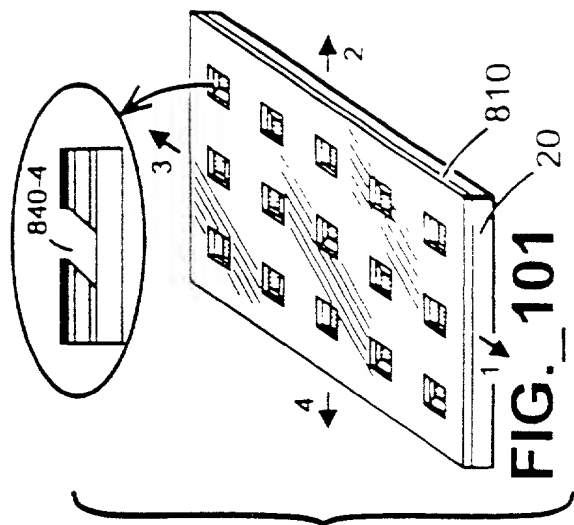
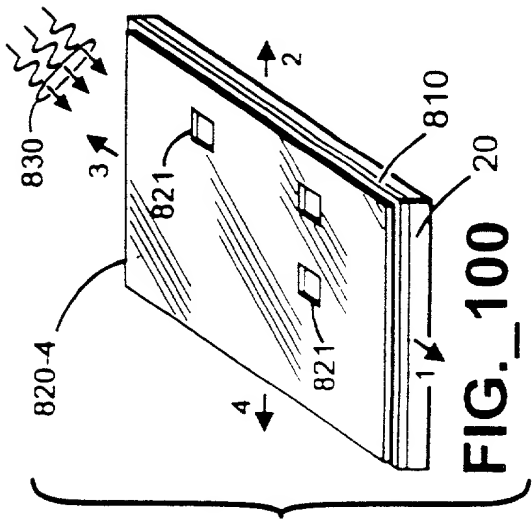
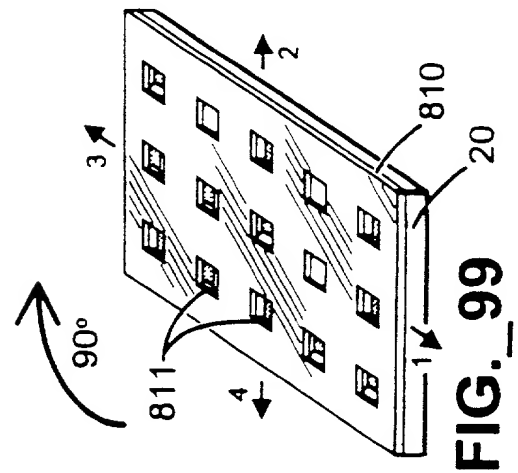
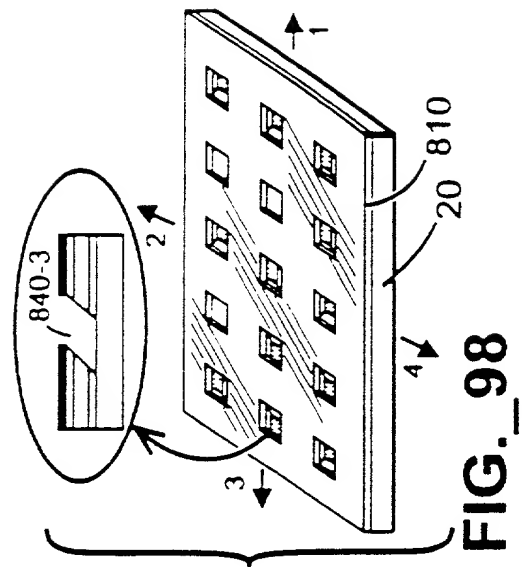
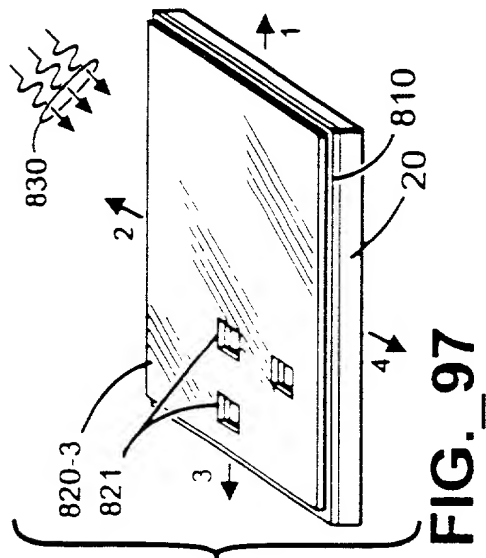
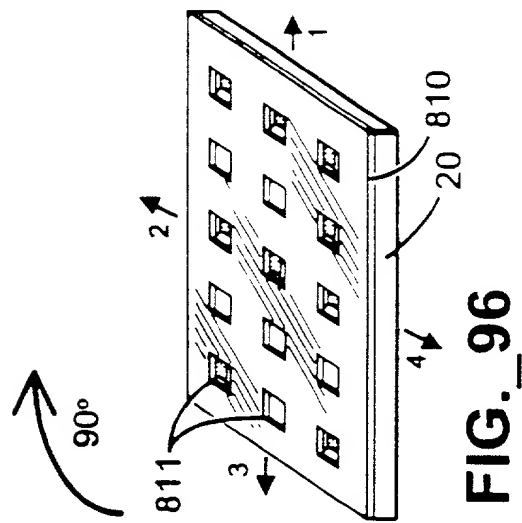


**FIG.\_76** (Transfer)



Substrate 12, Core 620, Clad coat 23





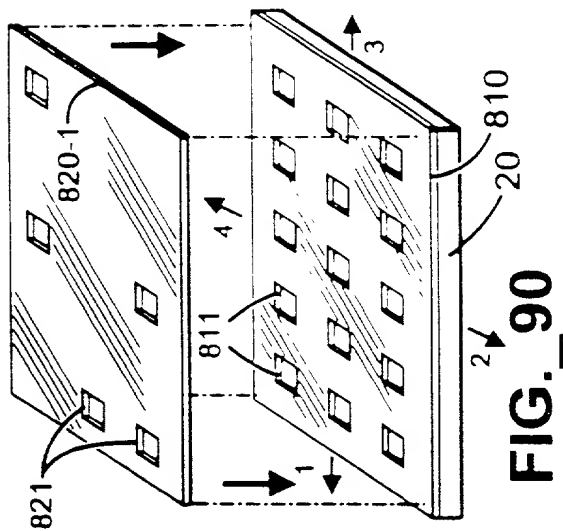


FIG. 90

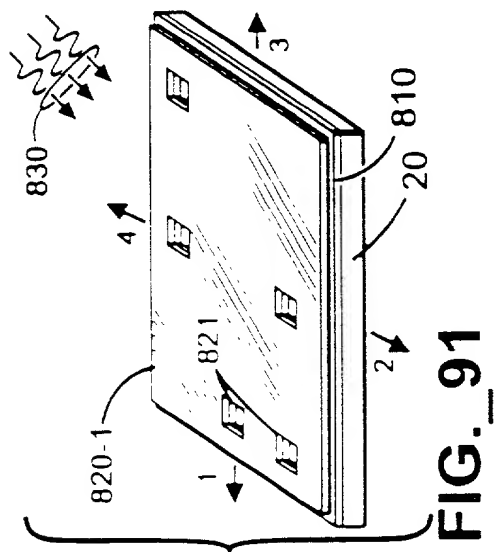


FIG. 91

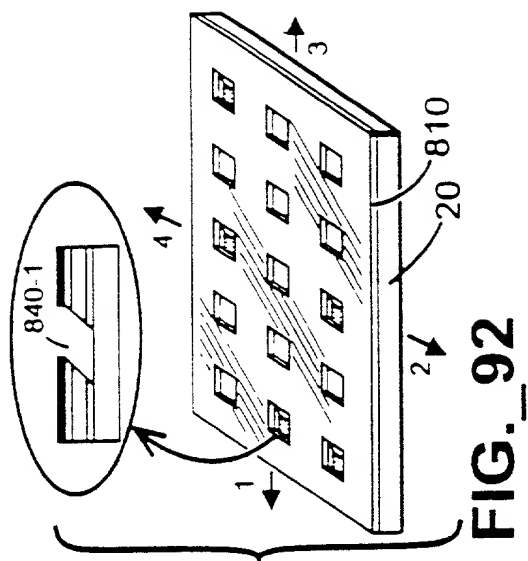


FIG. 92

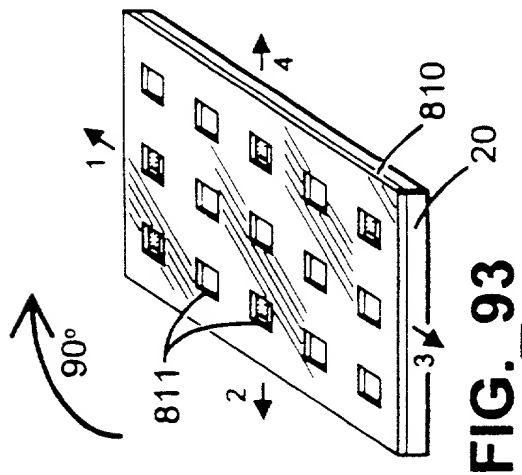


FIG. 93

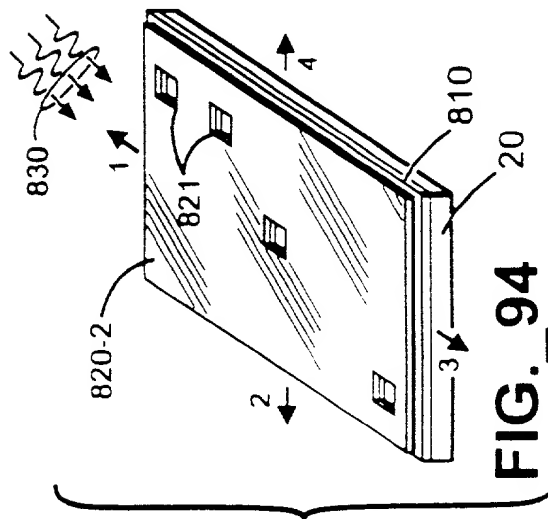


FIG. 94

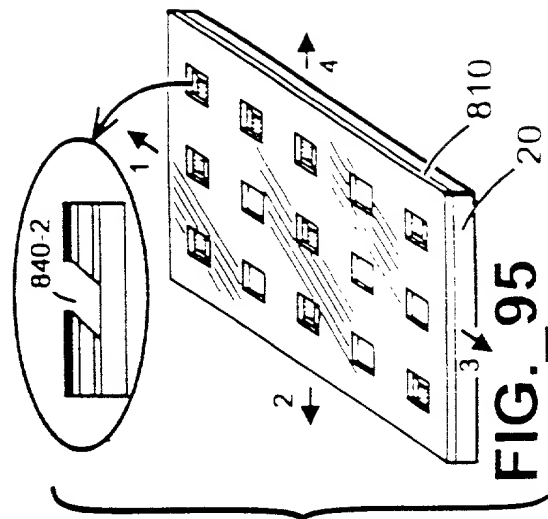
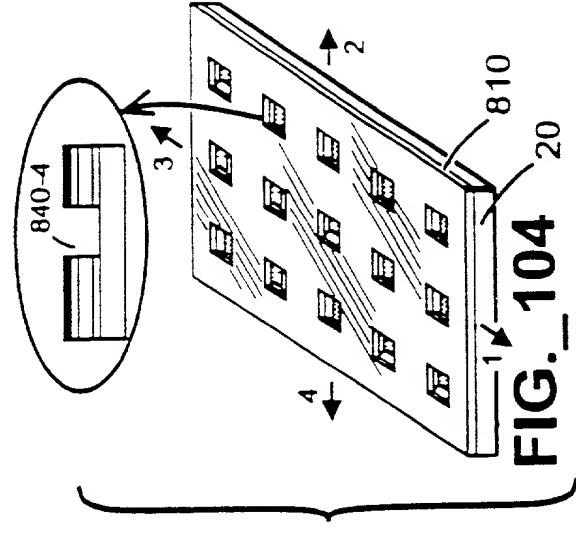
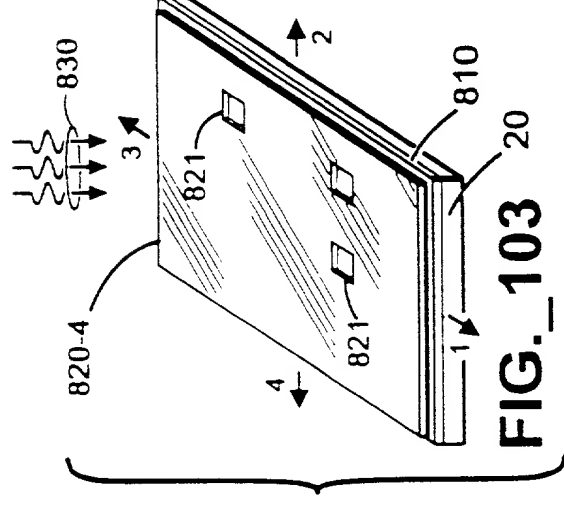
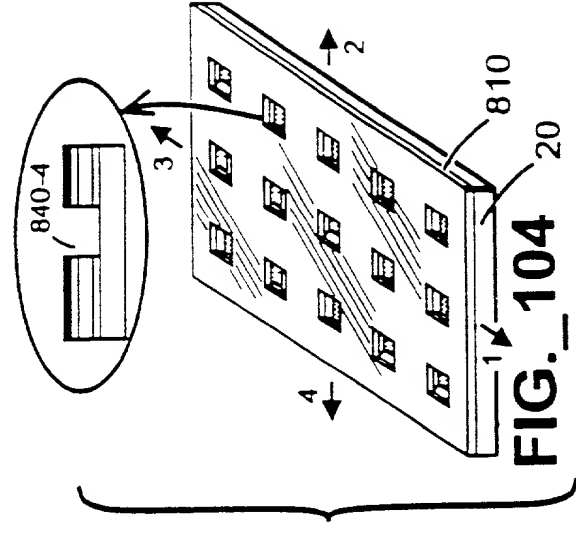


FIG. 95





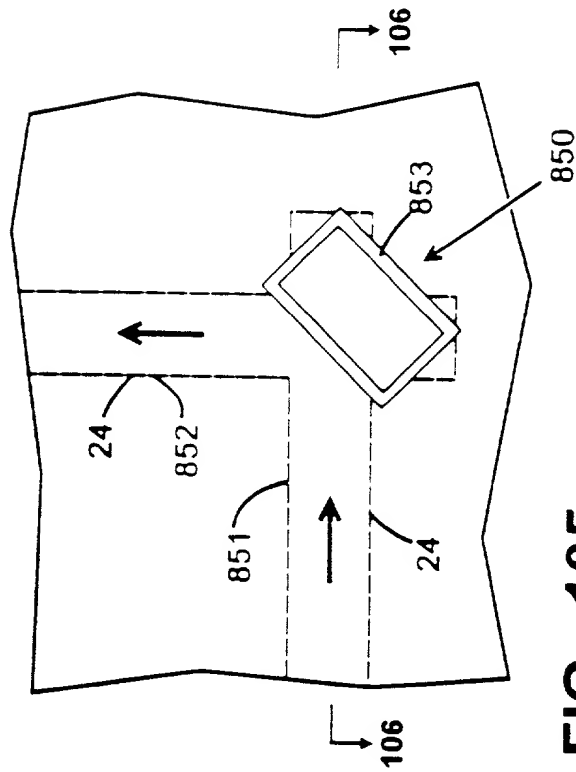


FIG. 105

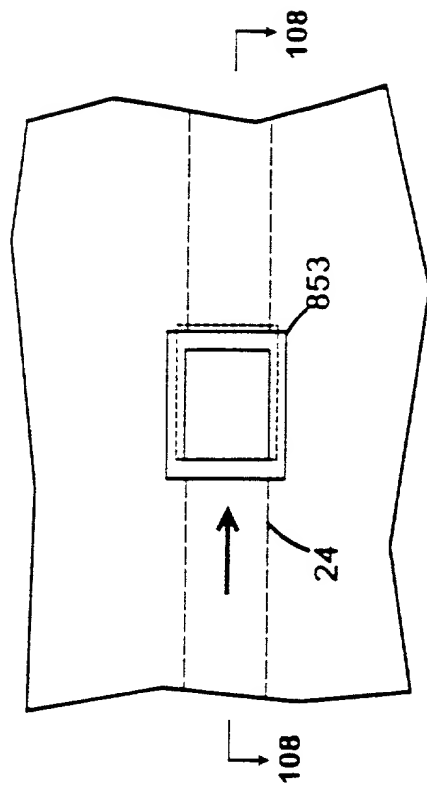


FIG. 107

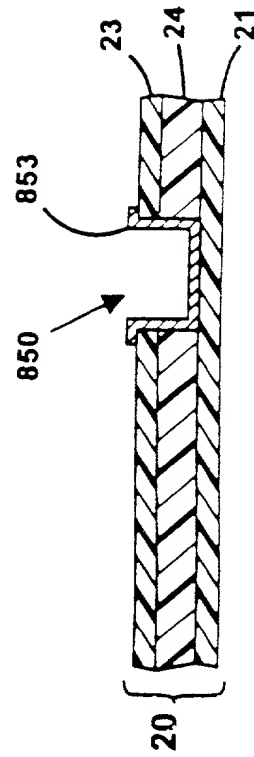


FIG. 106

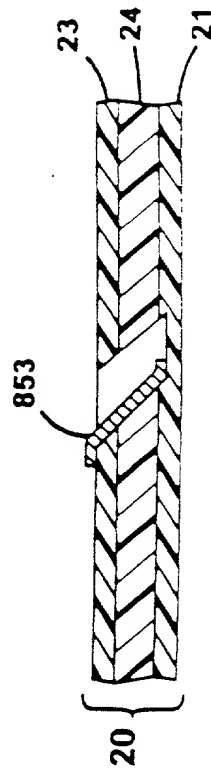
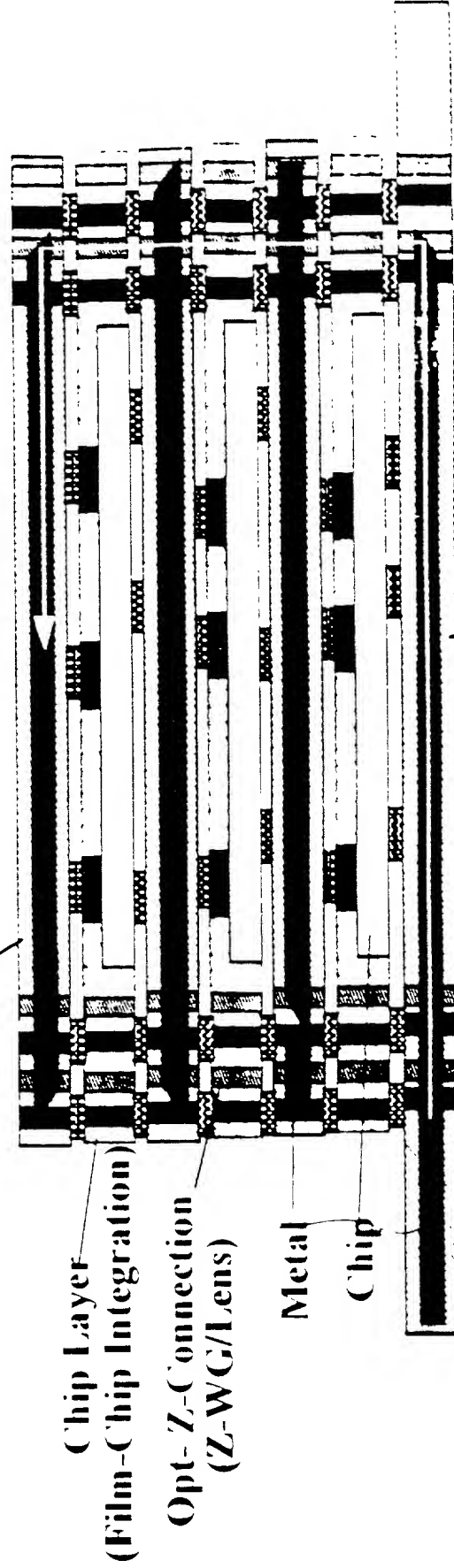


FIG. 108

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**GS CX/CXX OE Solution --- OE-3D-Stack**

OE-film-DW (I) or (M)



OE-film-DW

A 22

FIG. 109

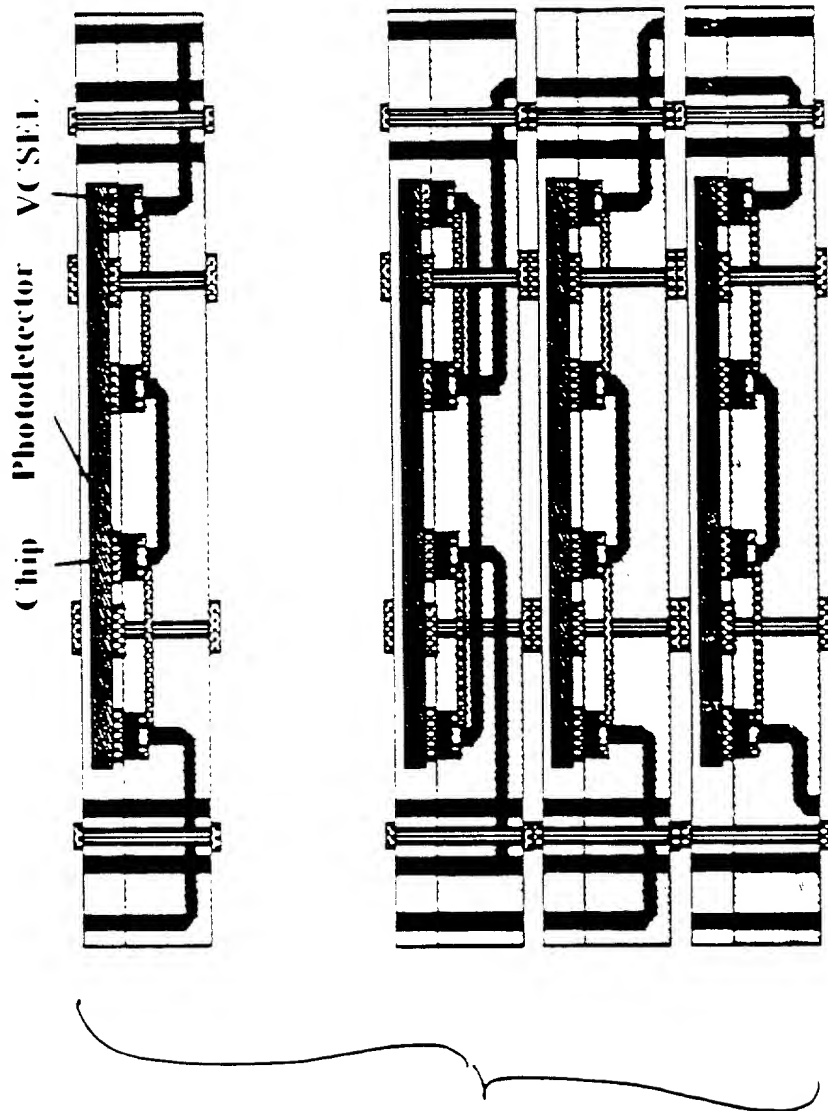


Fig. 110

A23

(2/23/99) AA1 Detail picture Example for 3D-stack'

(New version of the AA1 of 2/5/99)

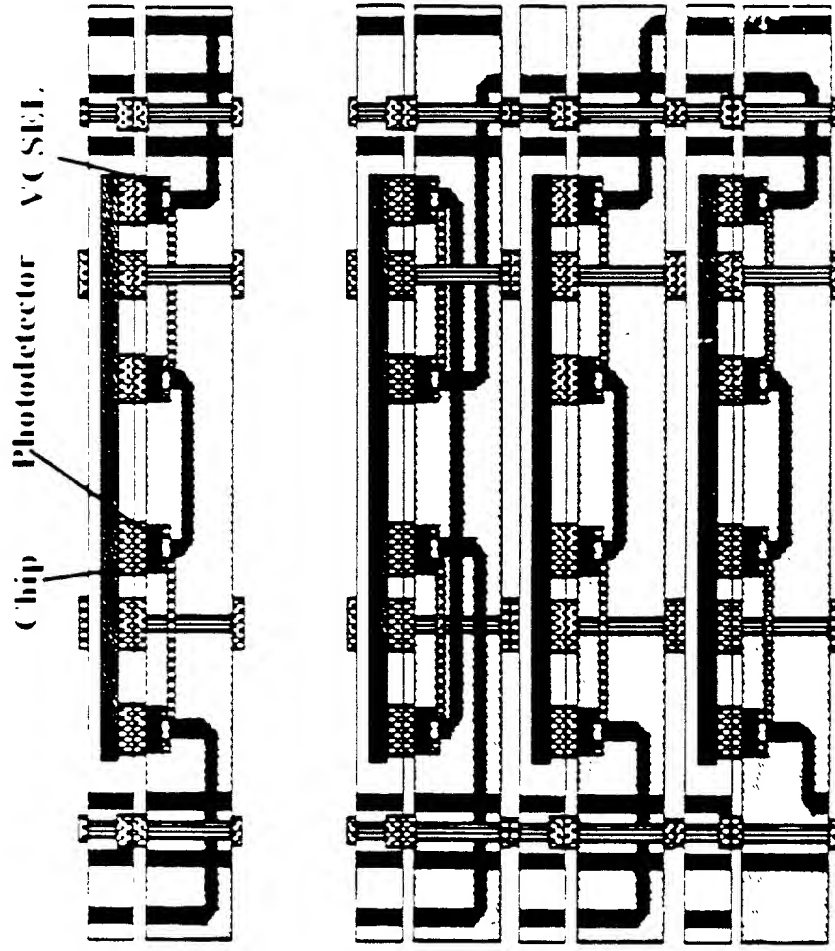


Fig. 110

(2/23/99) AA2 Detail picture Example for 3D-stack'

(New version of the AA2 of 2/5/99)

A24

Film/Z-Connection Application to OE-Substrate

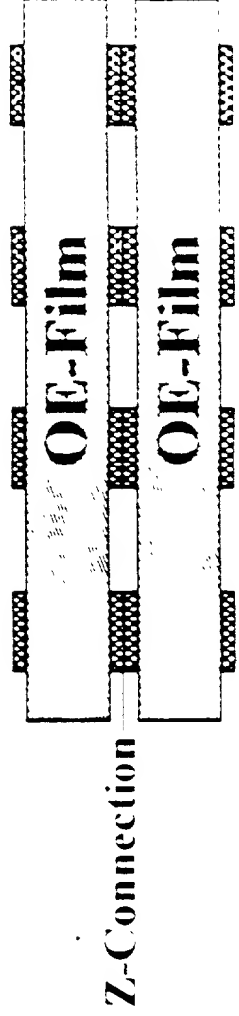
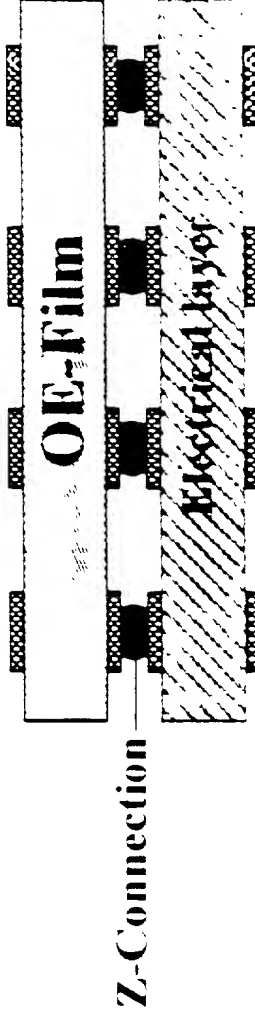
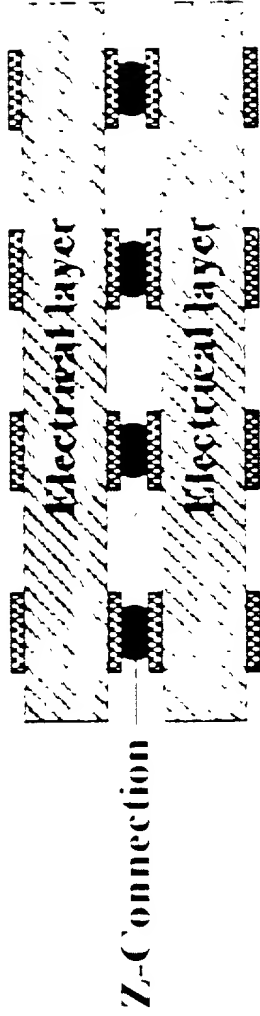
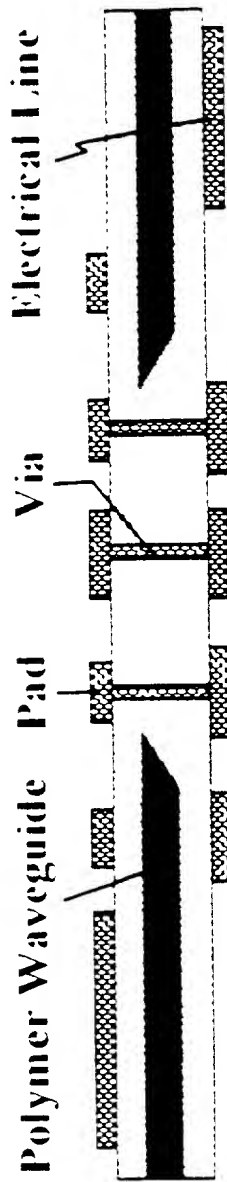


Fig. 1/2

A7

# OE-Films



OE-film-W

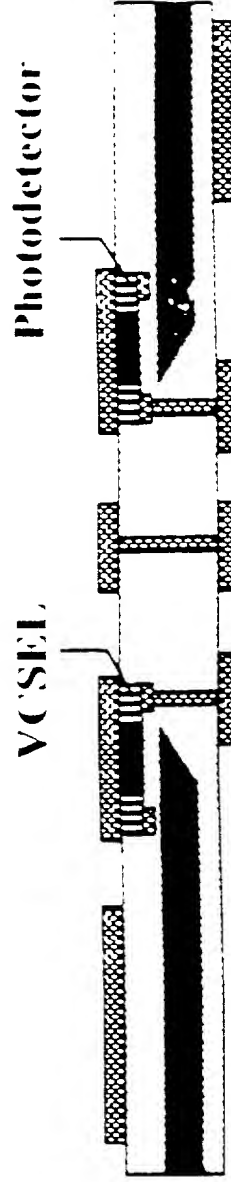
FIG. 113



OE-film-D

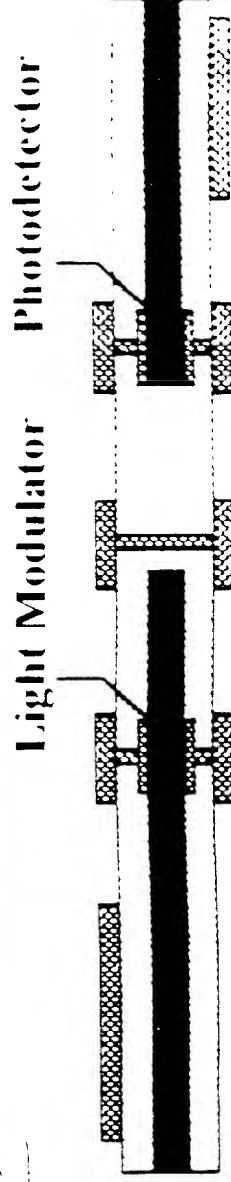
FIG. 114

A8



OE-film-DW(V)

FIG. 115



OE-film-DW(M)

2/17/99-added 2

FIG. 116

117

FOLM

Fiber Array  
Image Guide  
Waveguide Array

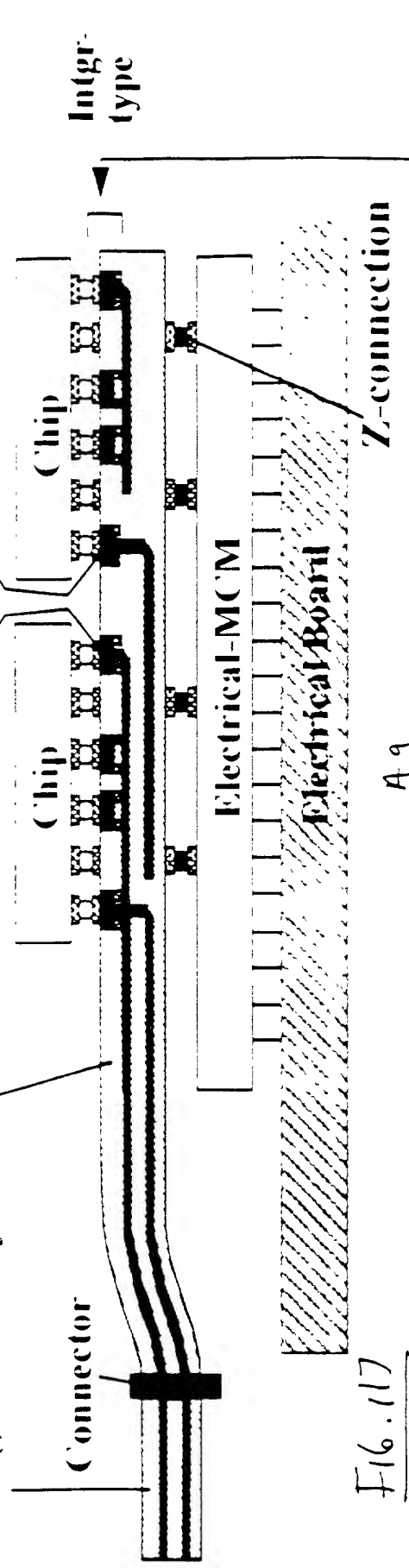
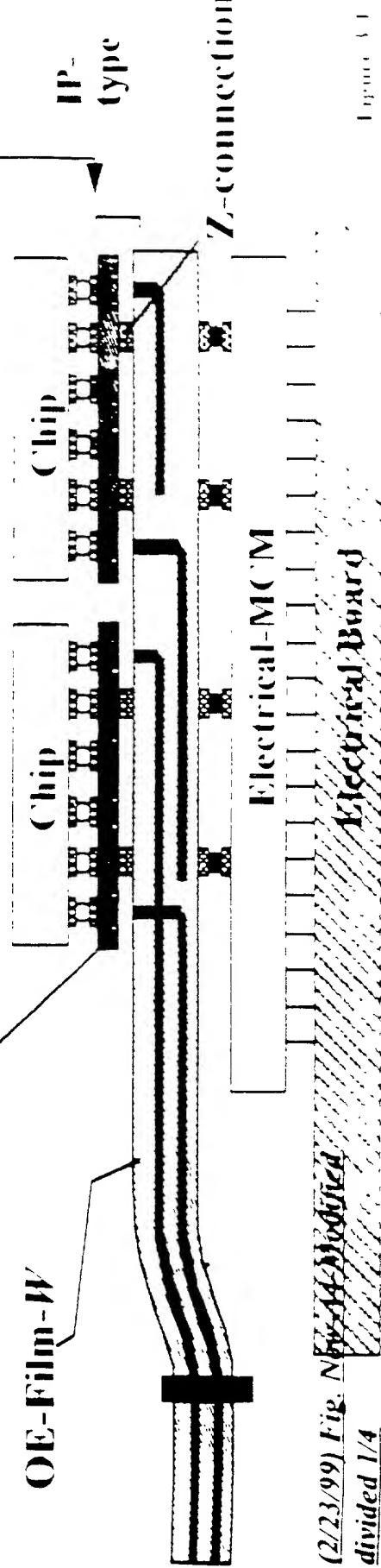


Fig. 117

OE-Film-D



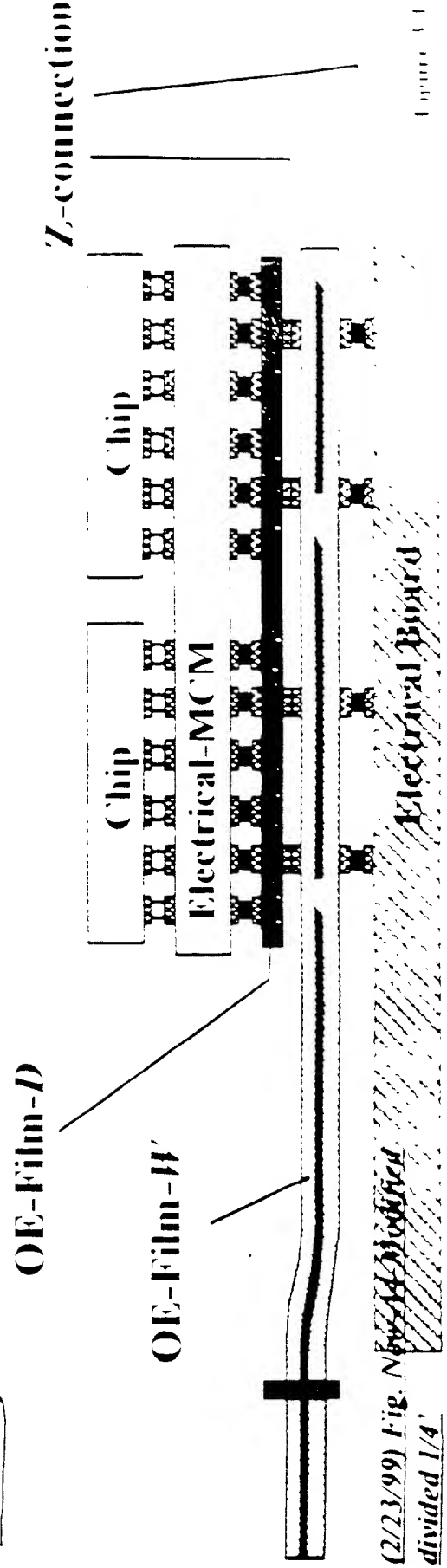
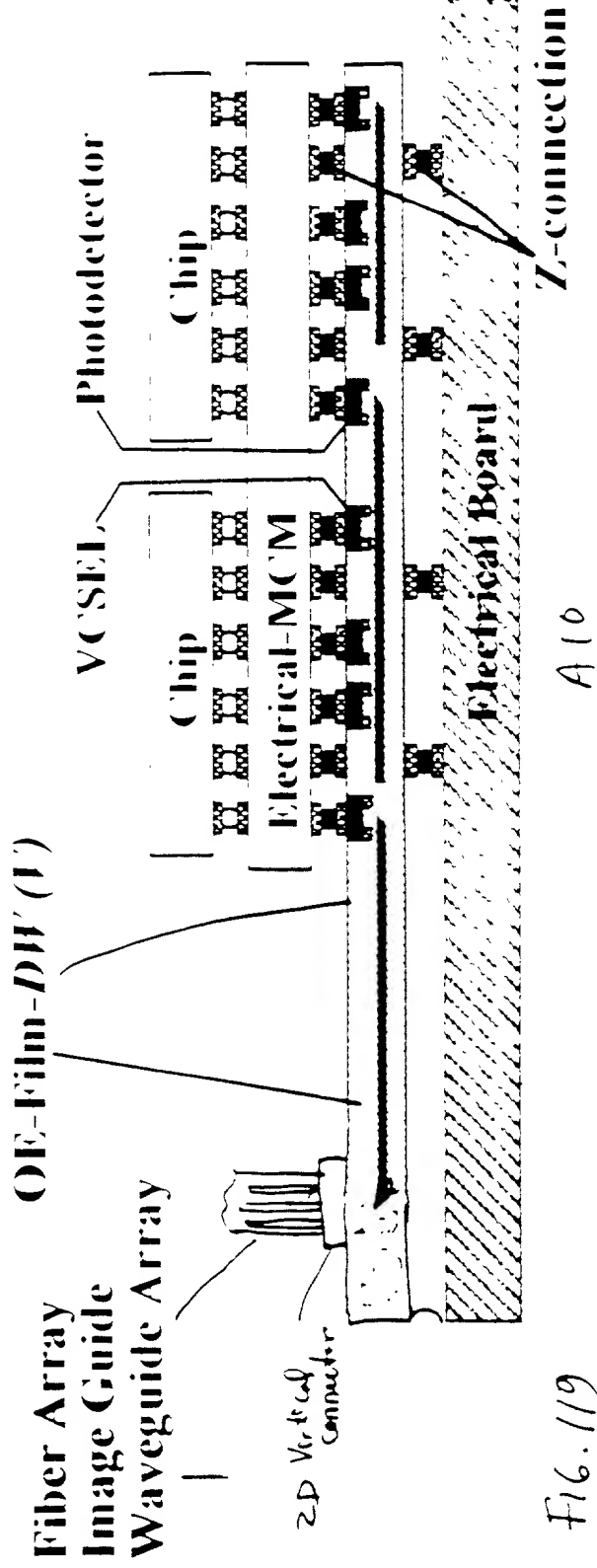
(2/23/99) Fig. No. 118 Modified  
divided 1/4

Fig. 118

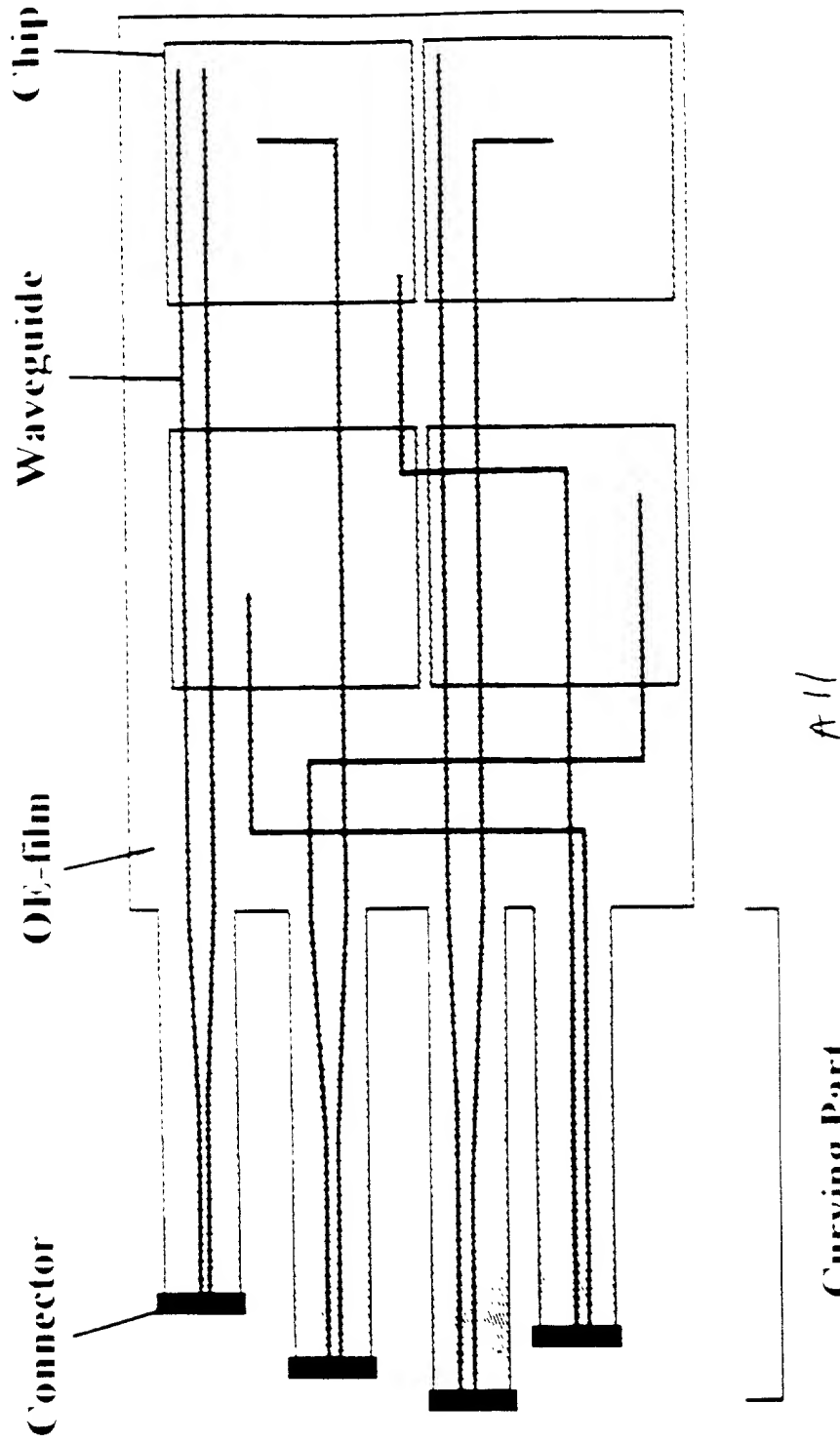
10 3/23/90



FOLM



**FUJITSU** Computer Packaging Technologies, Inc. **FCPT**  
**FOLM with Optical Path Length Controller, Connector Buffer**



Curving Part

FIG. 121

(2/17/99) Fig. New-A4-Modified  
 divided 2/4

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**FOLM with Optical Path Length Controller, Connector Buffer**

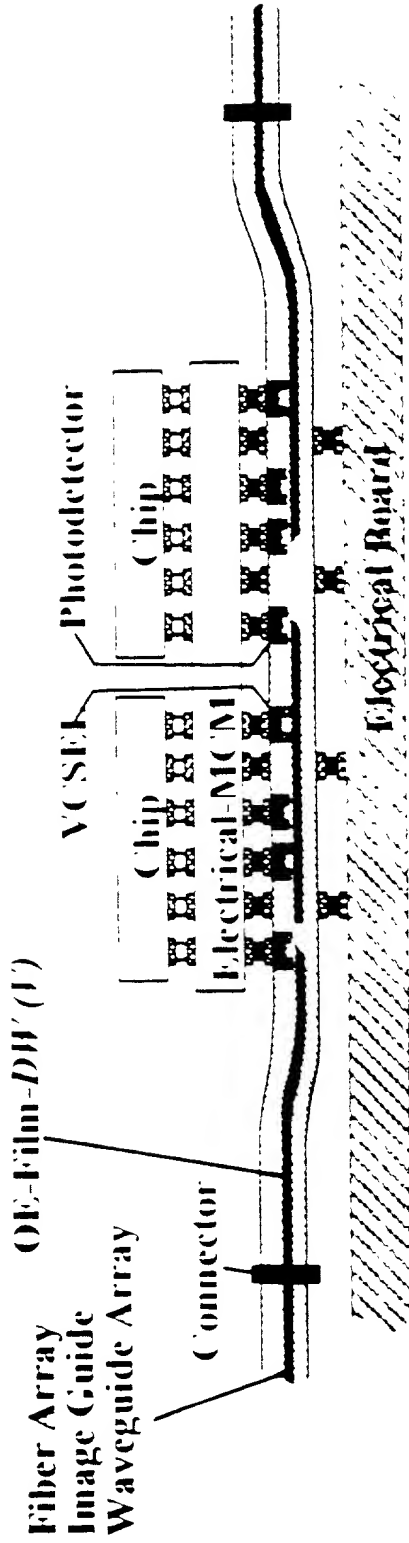


FIG. 123

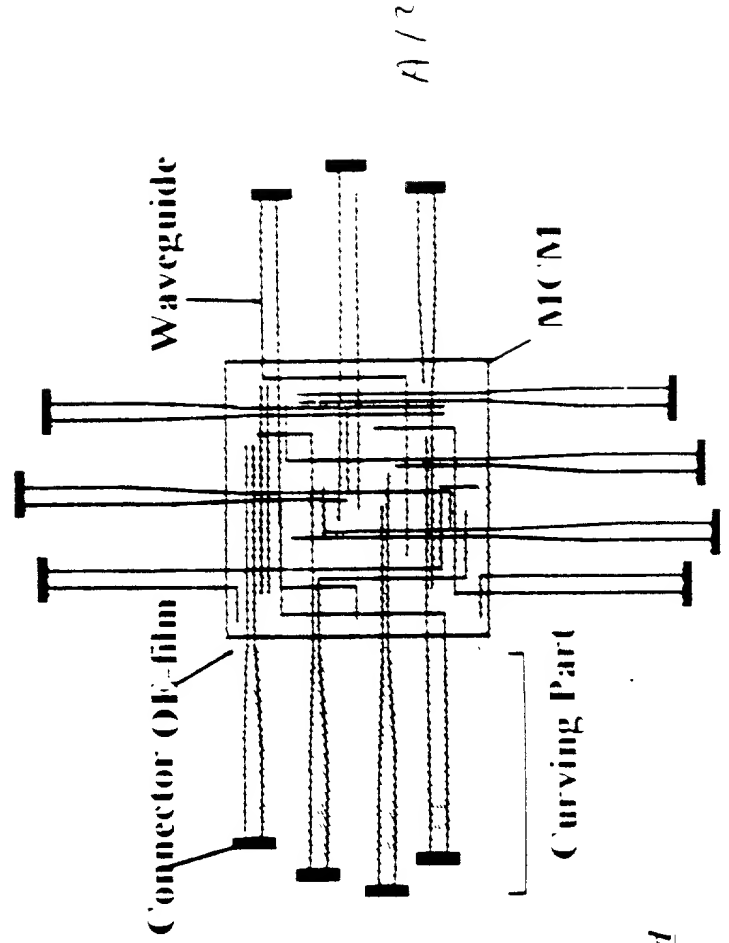
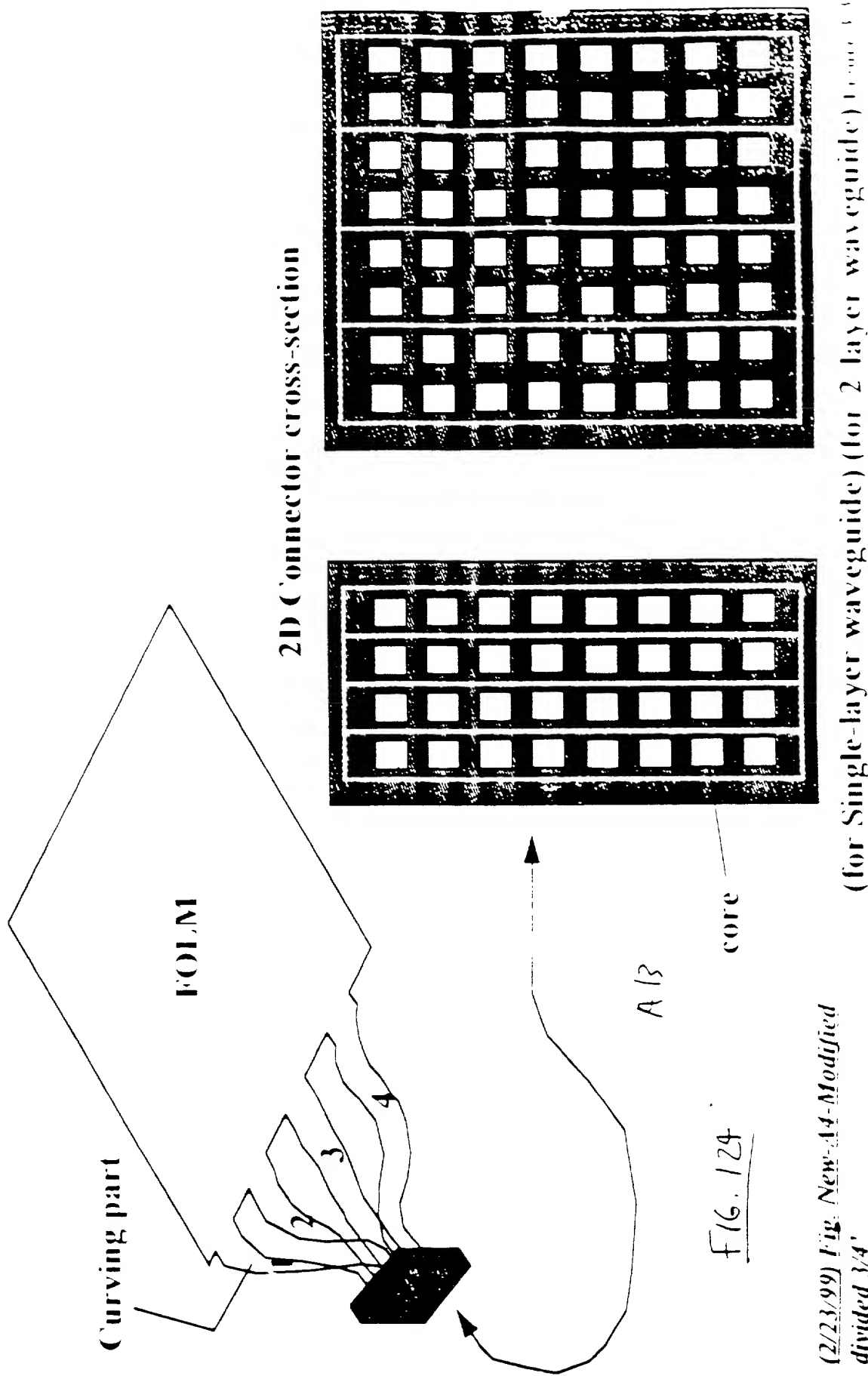


FIG. 122

(2/23/99) Fig. New-A4-Modified  
 divided 2/4'

# FOLM with 2D Waveguide Connector



(2/23/99) Fig. New-A4-Modified  
divided 3/4

# FOLM: High-Speed Option

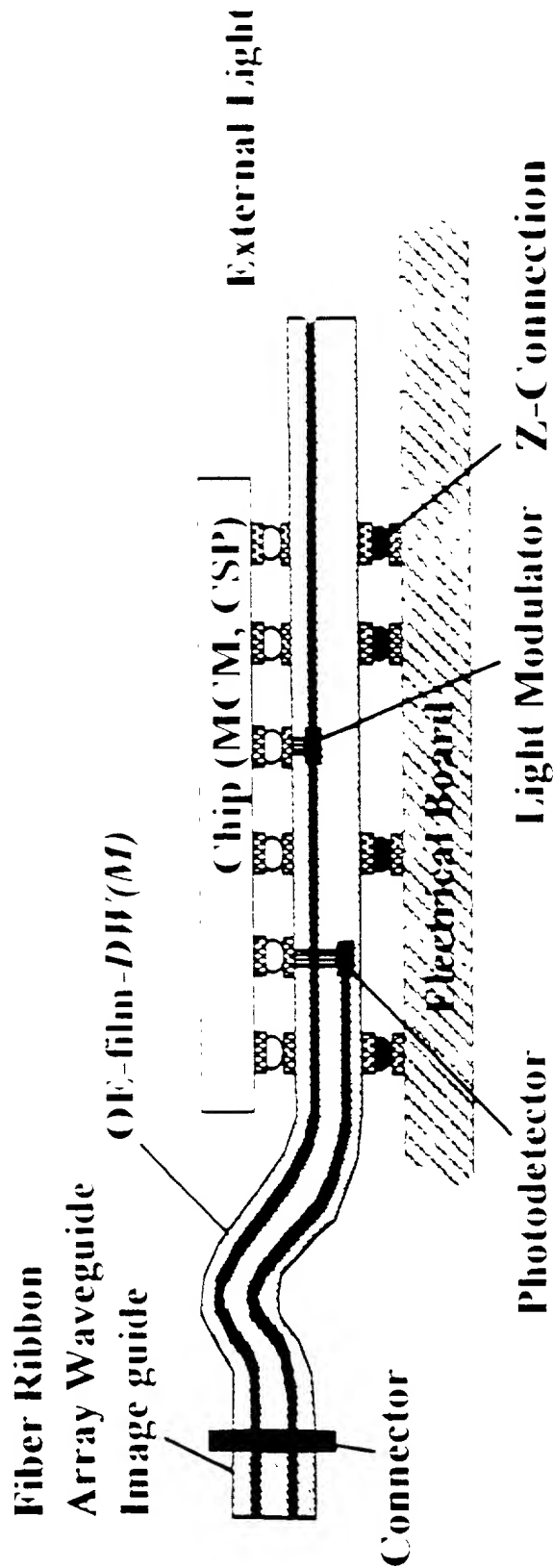
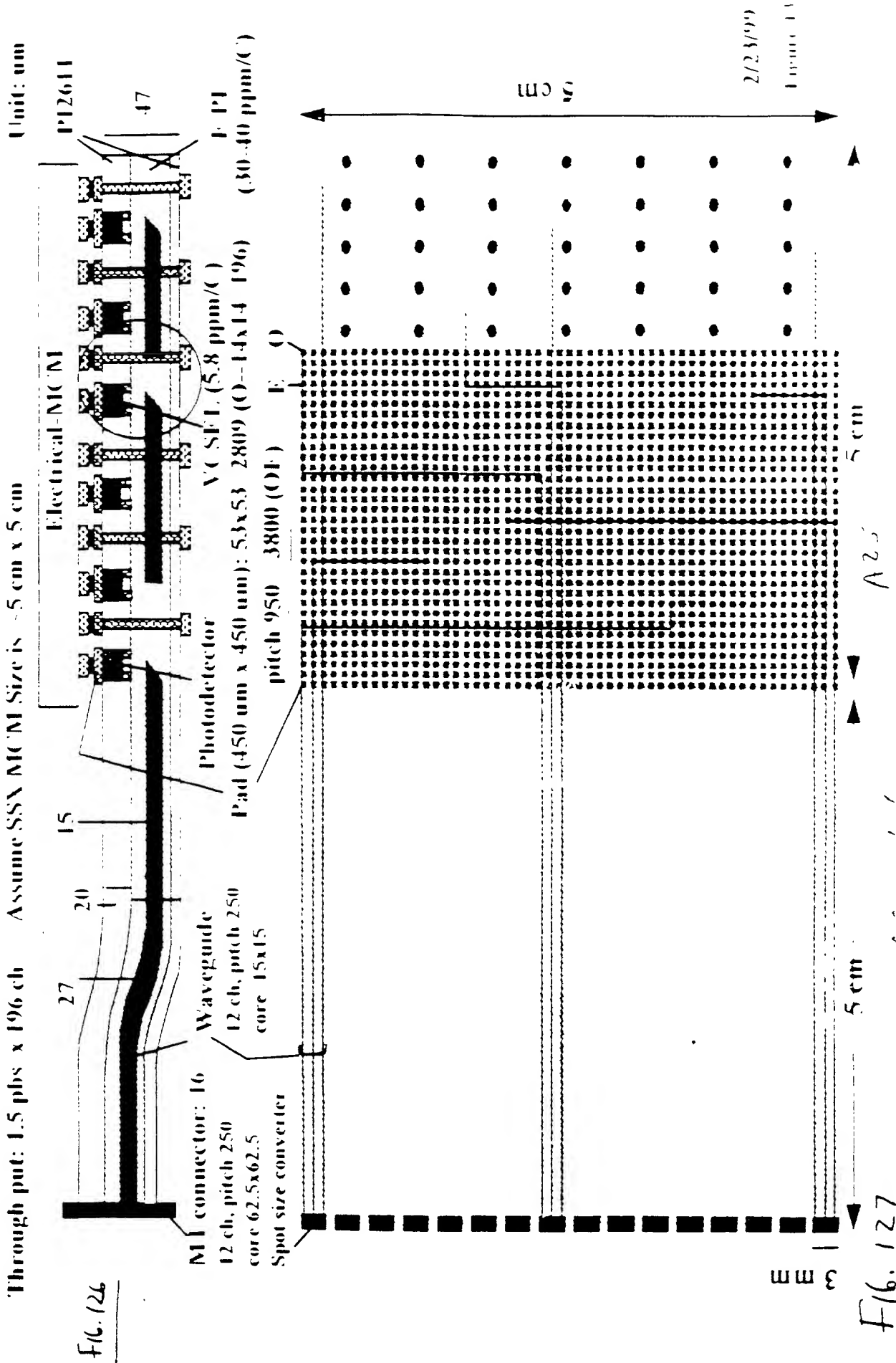


Fig. 125

A 14

# FOLM Structure Example (Overall)



FUJITSU Computer Packaging Technologies, Inc. FCPT  
FCOLM Structure Example (VCSEL part)

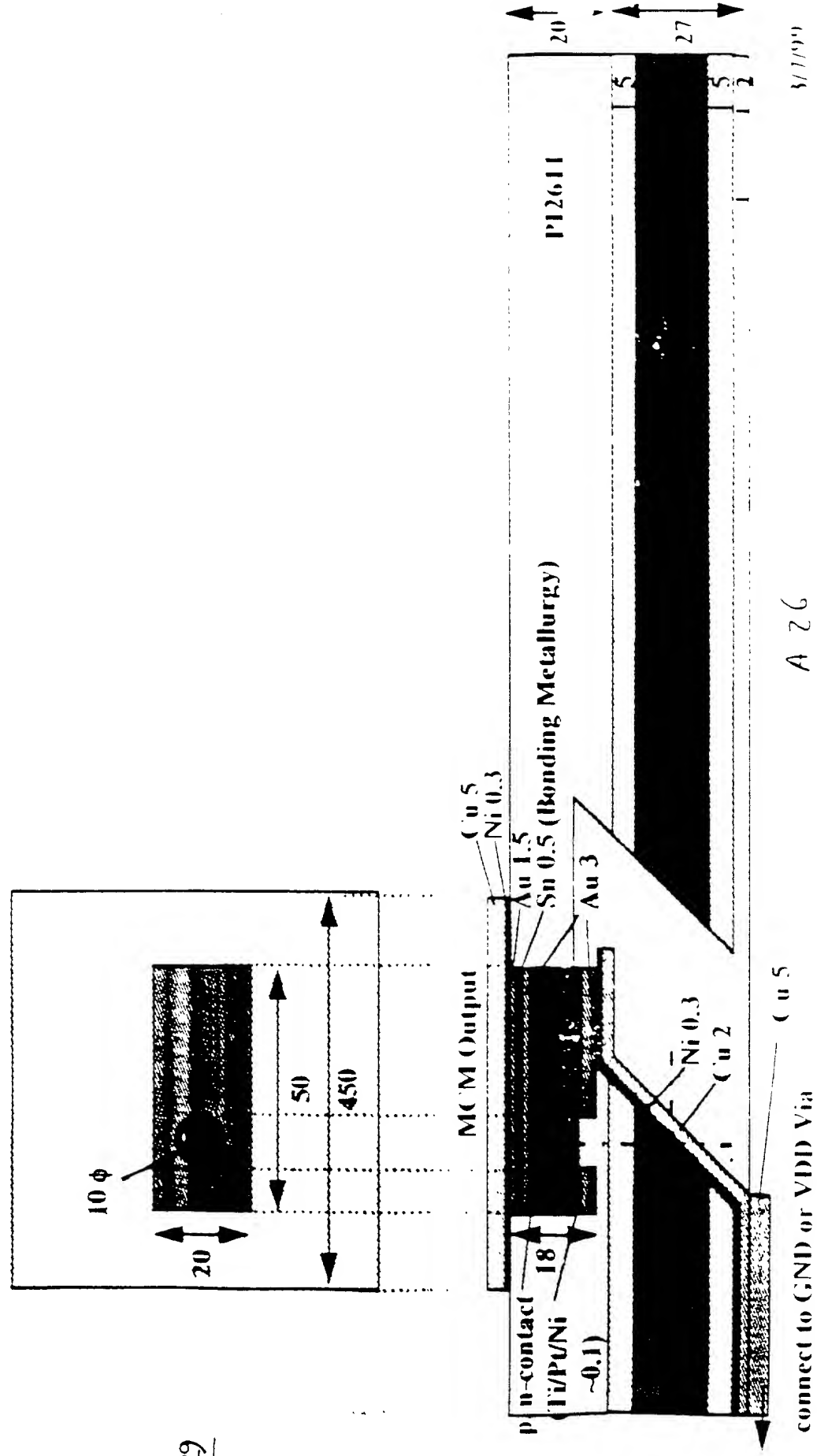


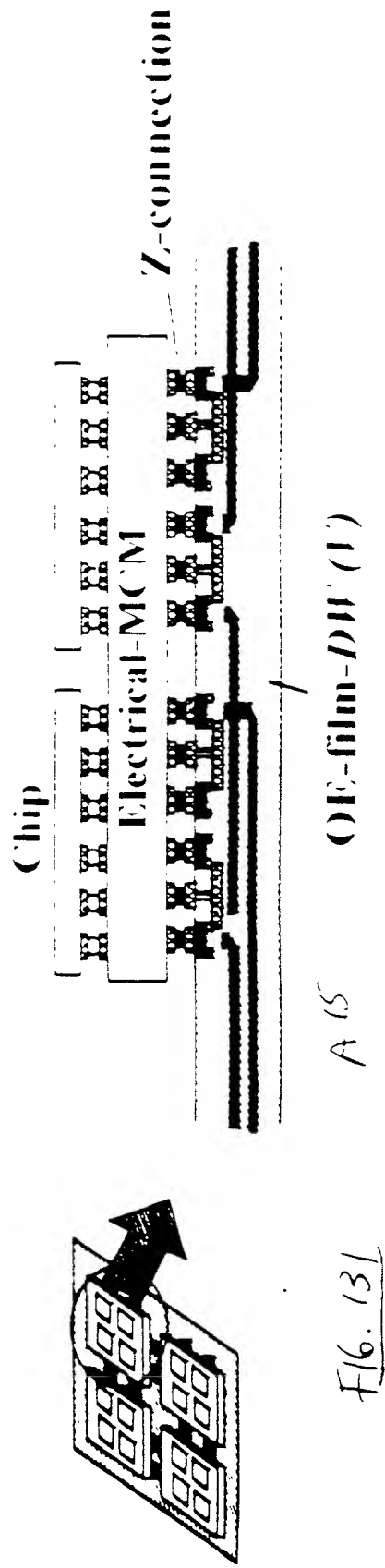
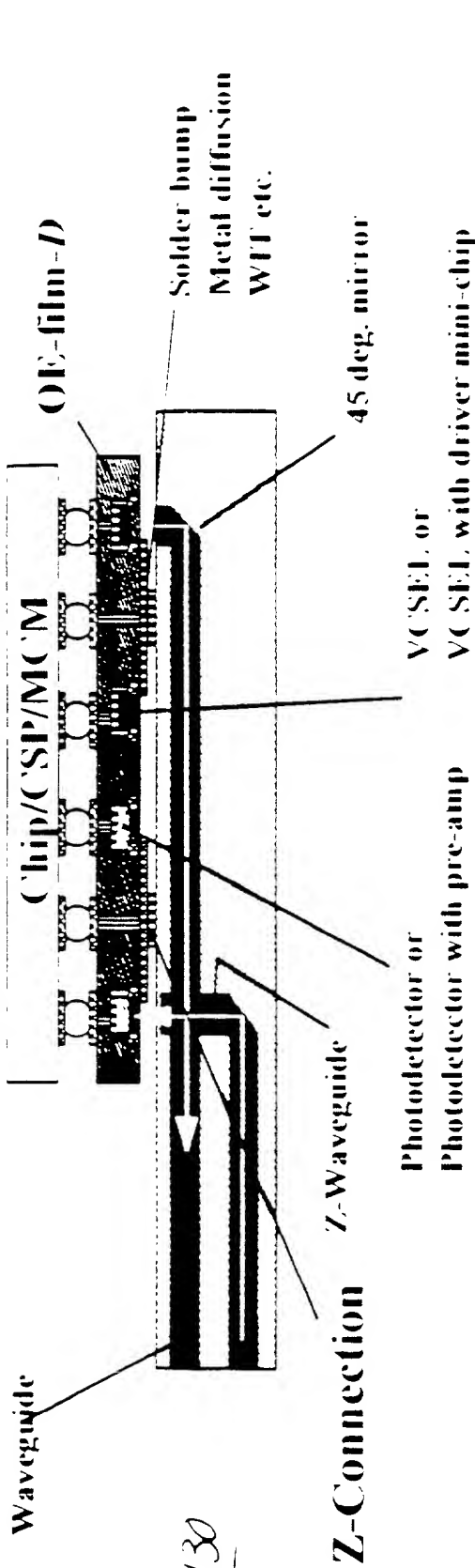
Fig. 128

Unit : mm

A 26

3/1/99

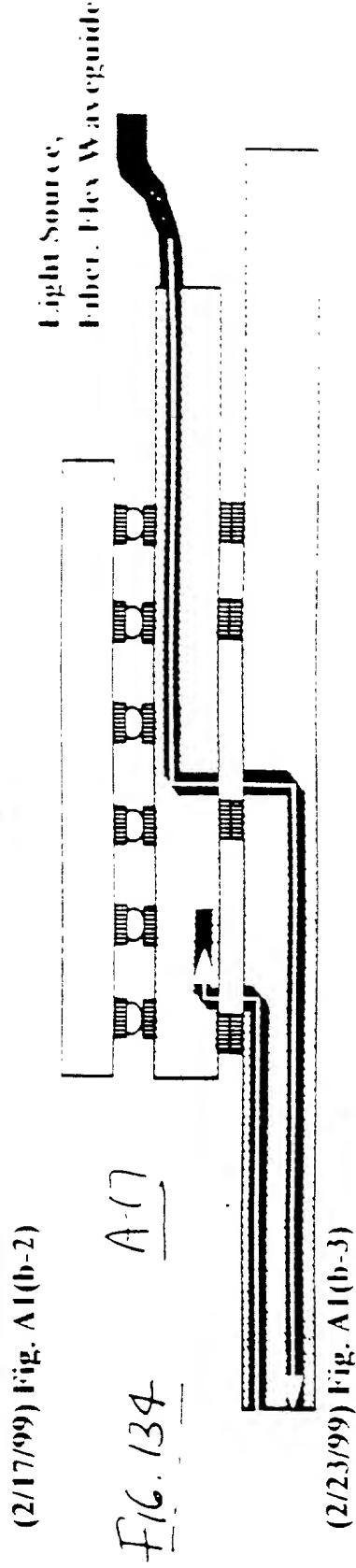
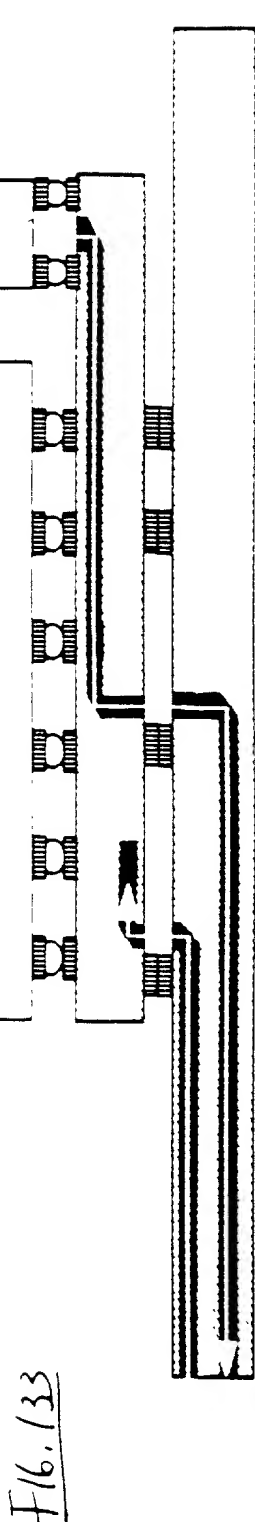
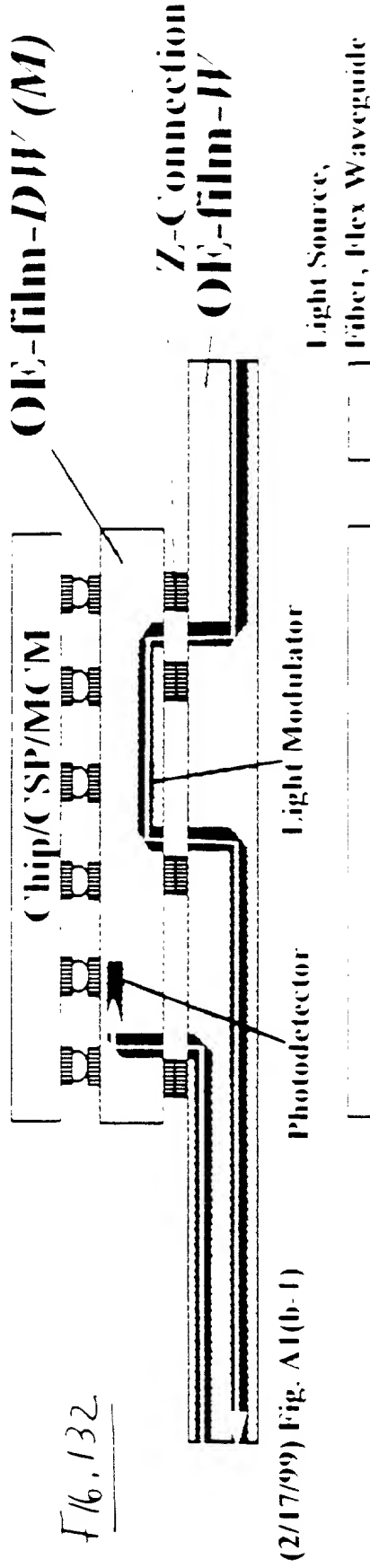
OE-film: OE-IP, OE-Film-MCM



(2/23/99) Fig. New-A1-Modified

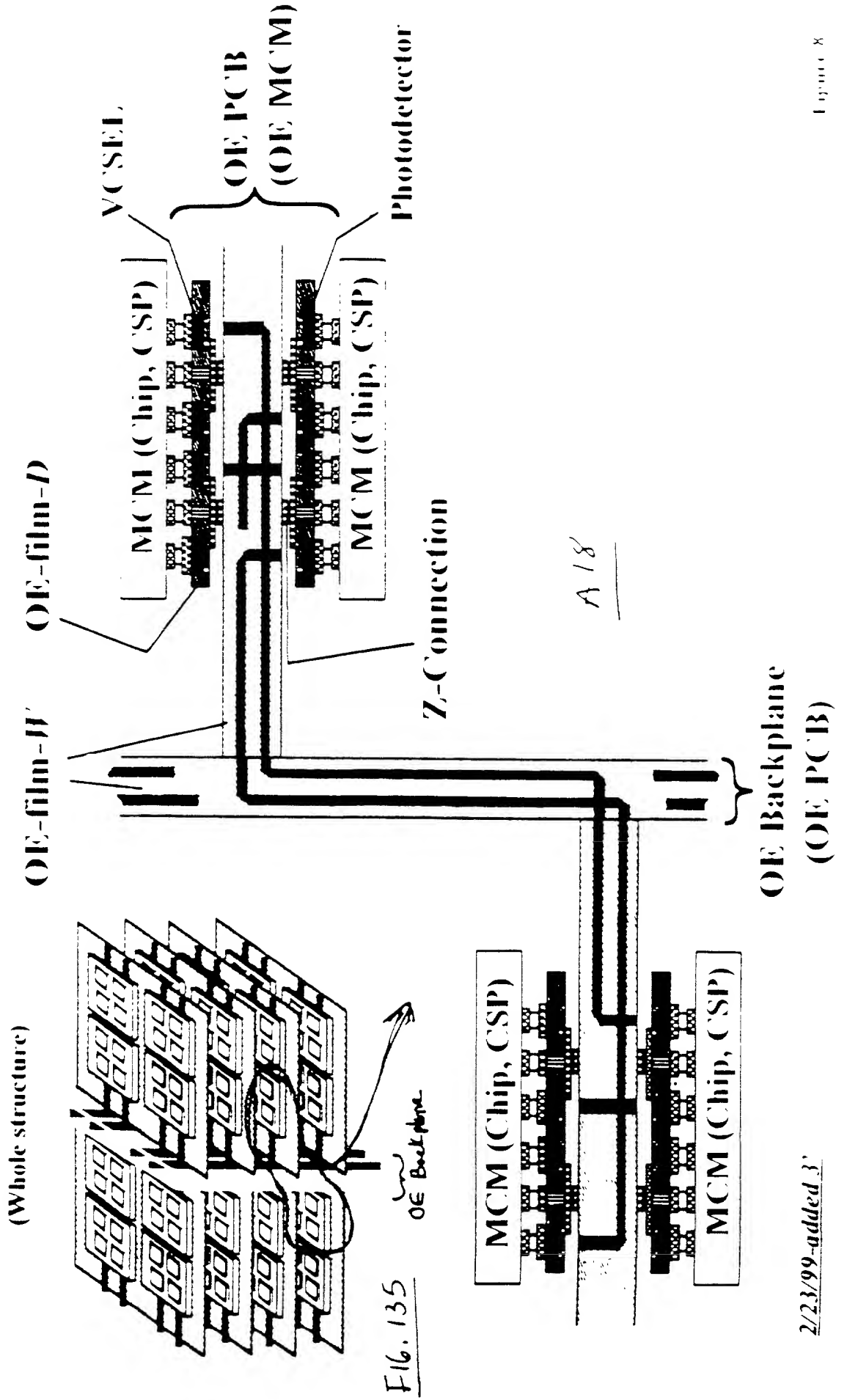


OE-film: Light Modulator Transmitters

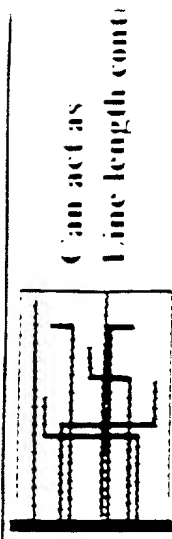


Examples of Light Modulators: Electro-Optic (EO) Modulator, Electro-Absorption (EA) Modulator

# OE-film: Both-Side Packaging



# Direct Jump from LSI



Fiber Ribbon Film Waveguide with Device Integration

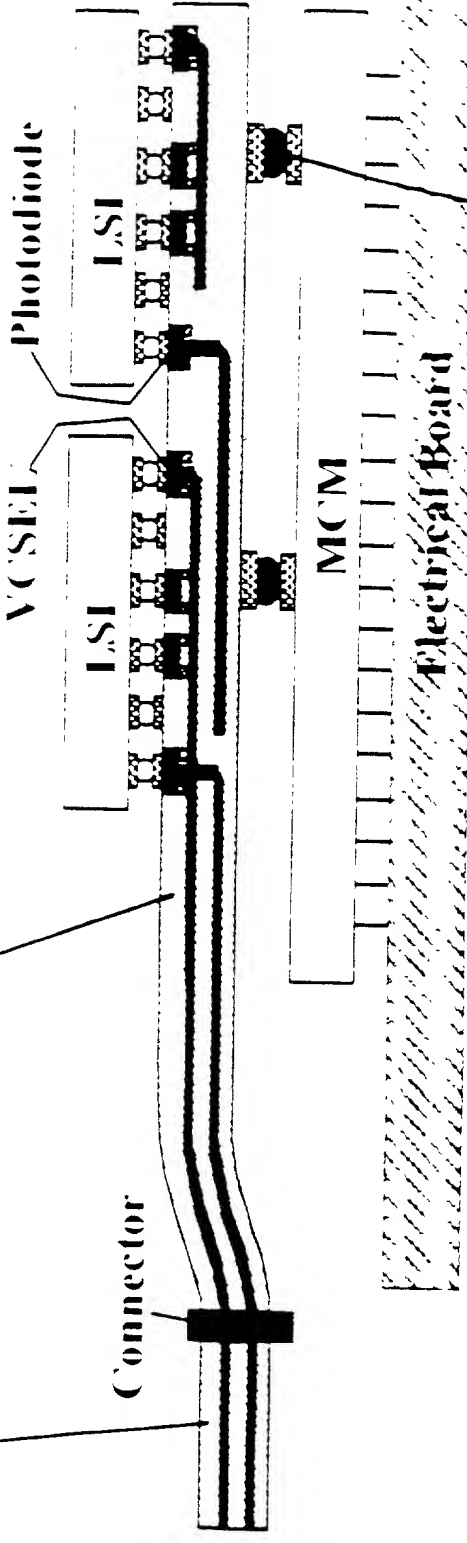


Fig. 136

Z-Connection

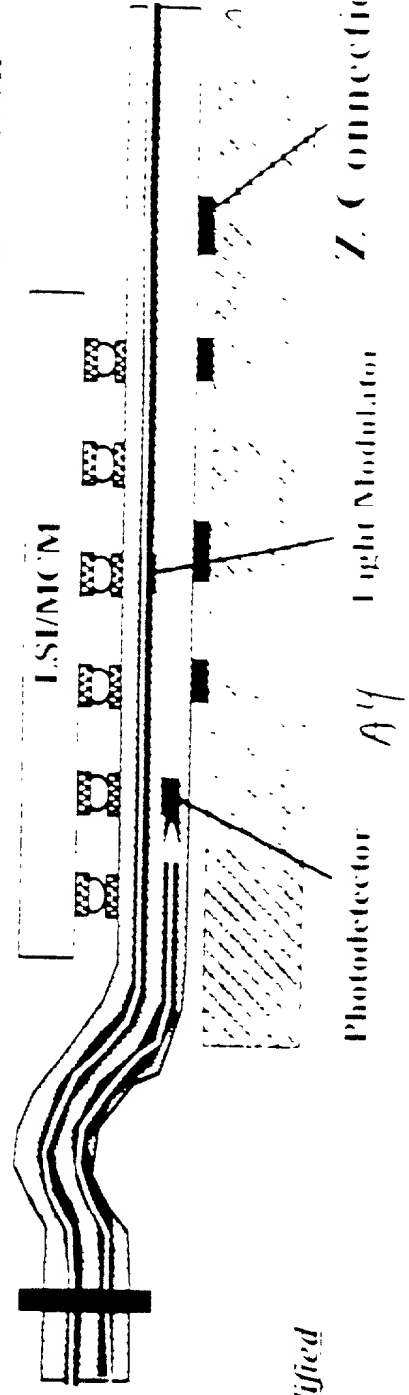
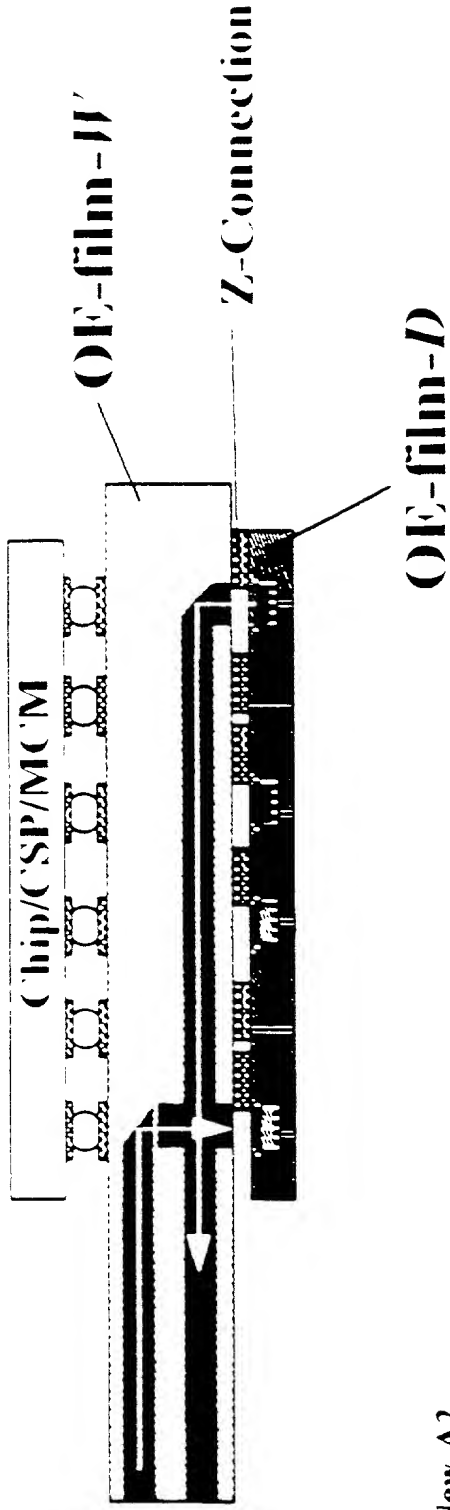


Fig. 137

Fig. New-44-Modified

OE IP is Placed on the Oposit Side

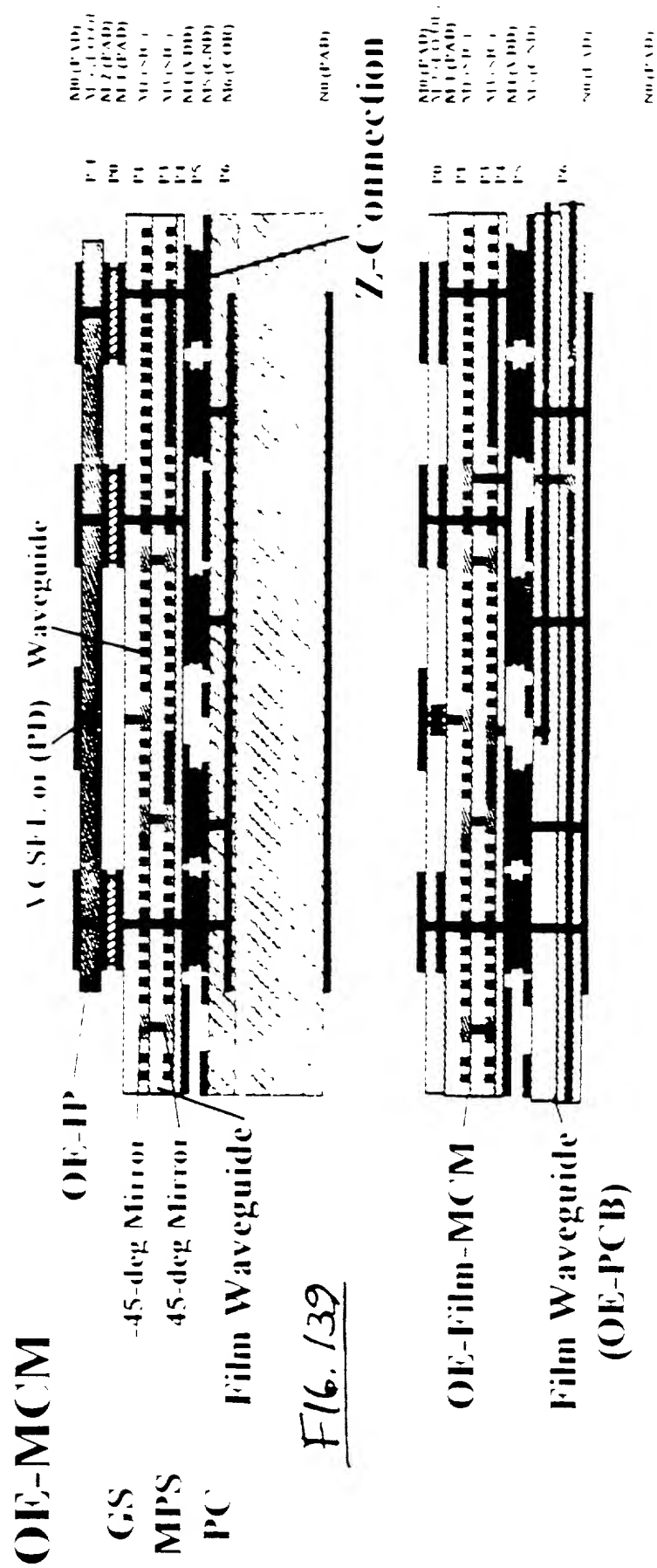


(2/23/99) Fig. New-A2

FL6.138

A2°

OE MCM



AS

Fig. A5-Modific

AS 1/18/99

OE-film: Smart Pixel



Fig 141

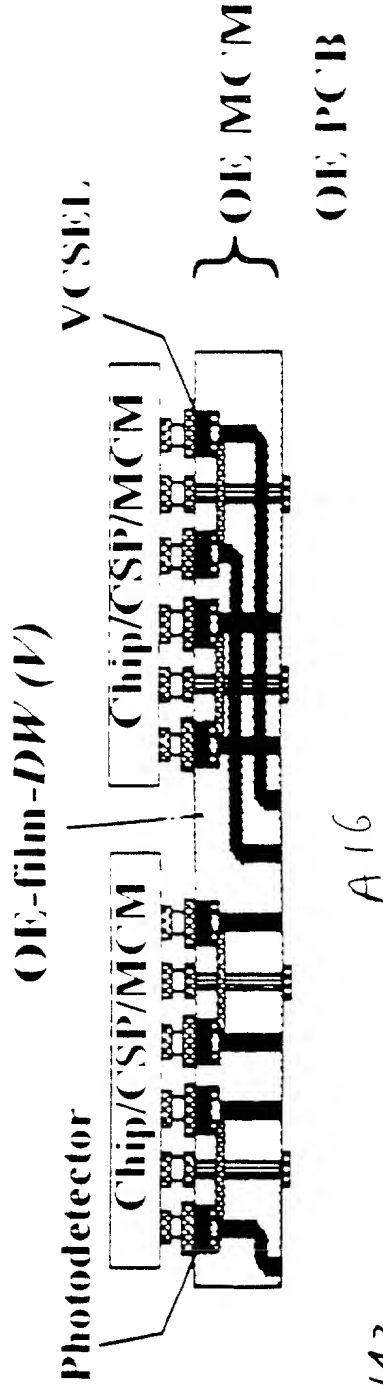


Fig. 142

# OE-Film/OE-Film Stack --- Back-Side Connection

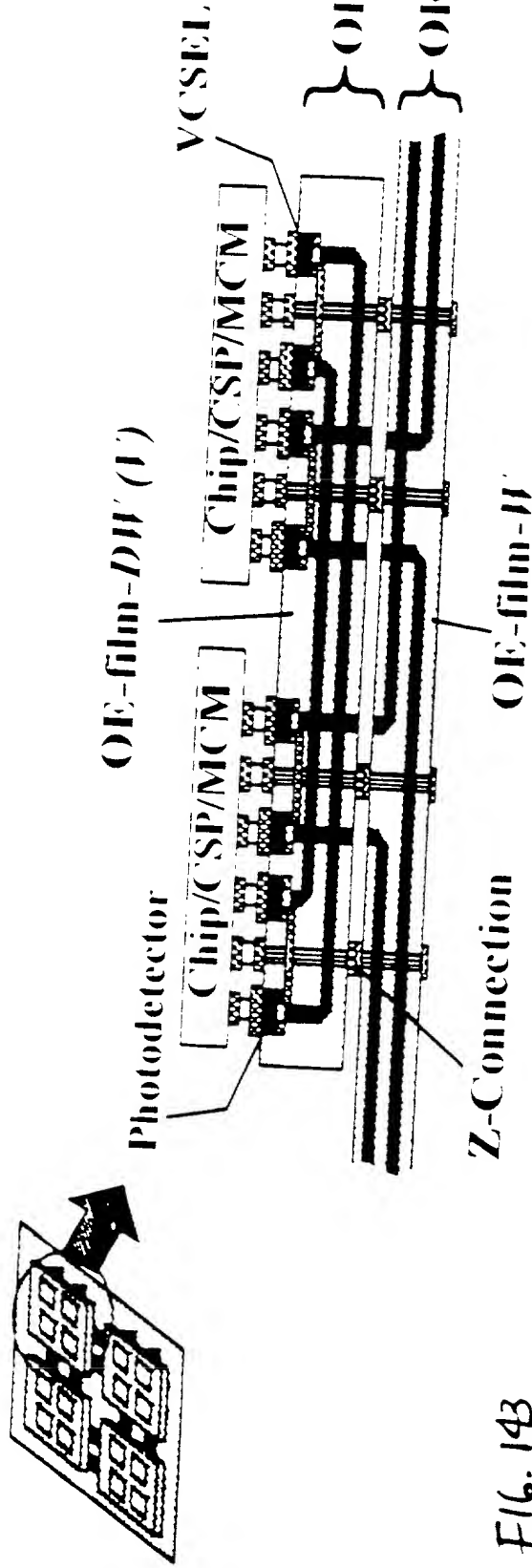


FIG. 14B

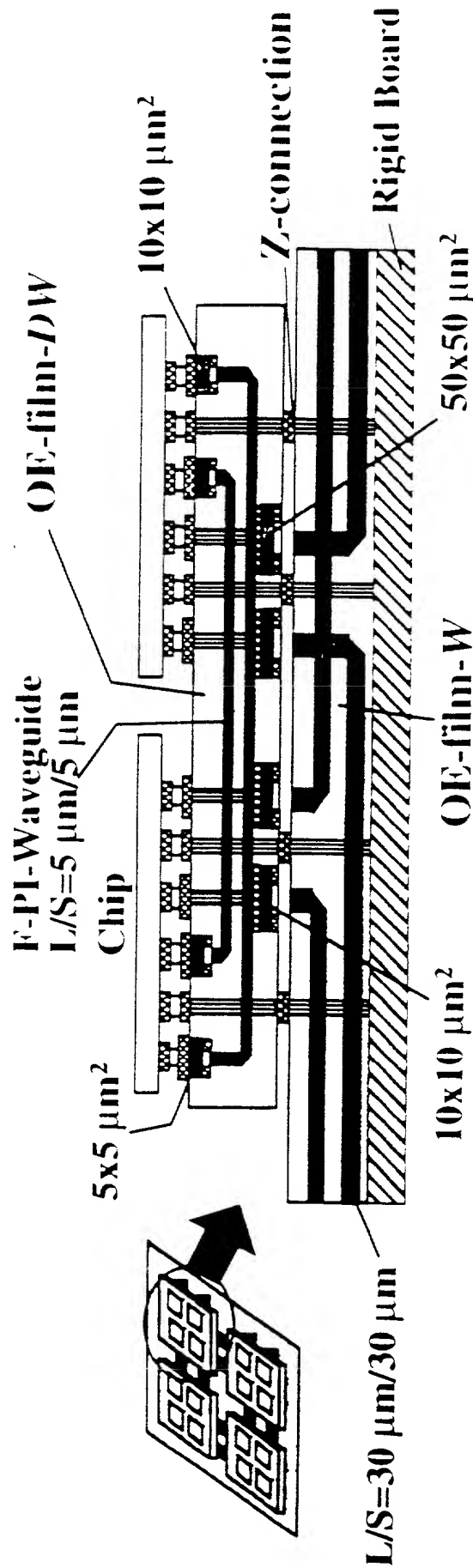
A19

2/23/99-added 4'

A19 2/7/99

Figure 9

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**OE-Film/OE-Film Stack --- Back-Side Connection**



DI

FIG 144

3/7

Fig. 3/18/99-1

DI 3/18/99



# OE-MCM/OE-Bord Stack

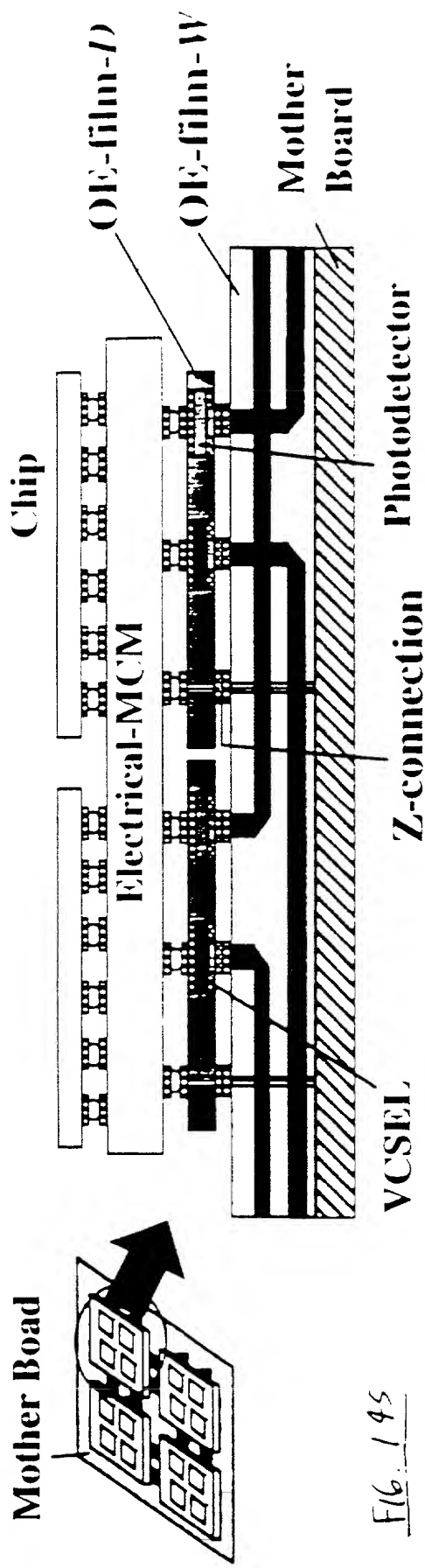


Fig. 145

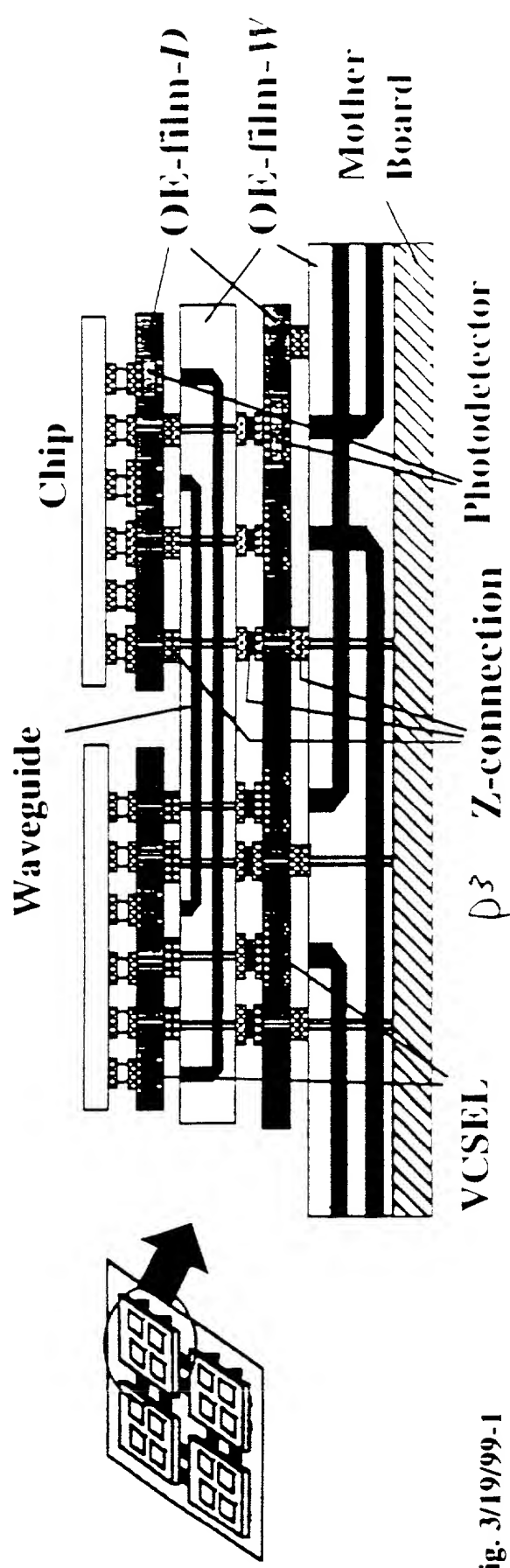
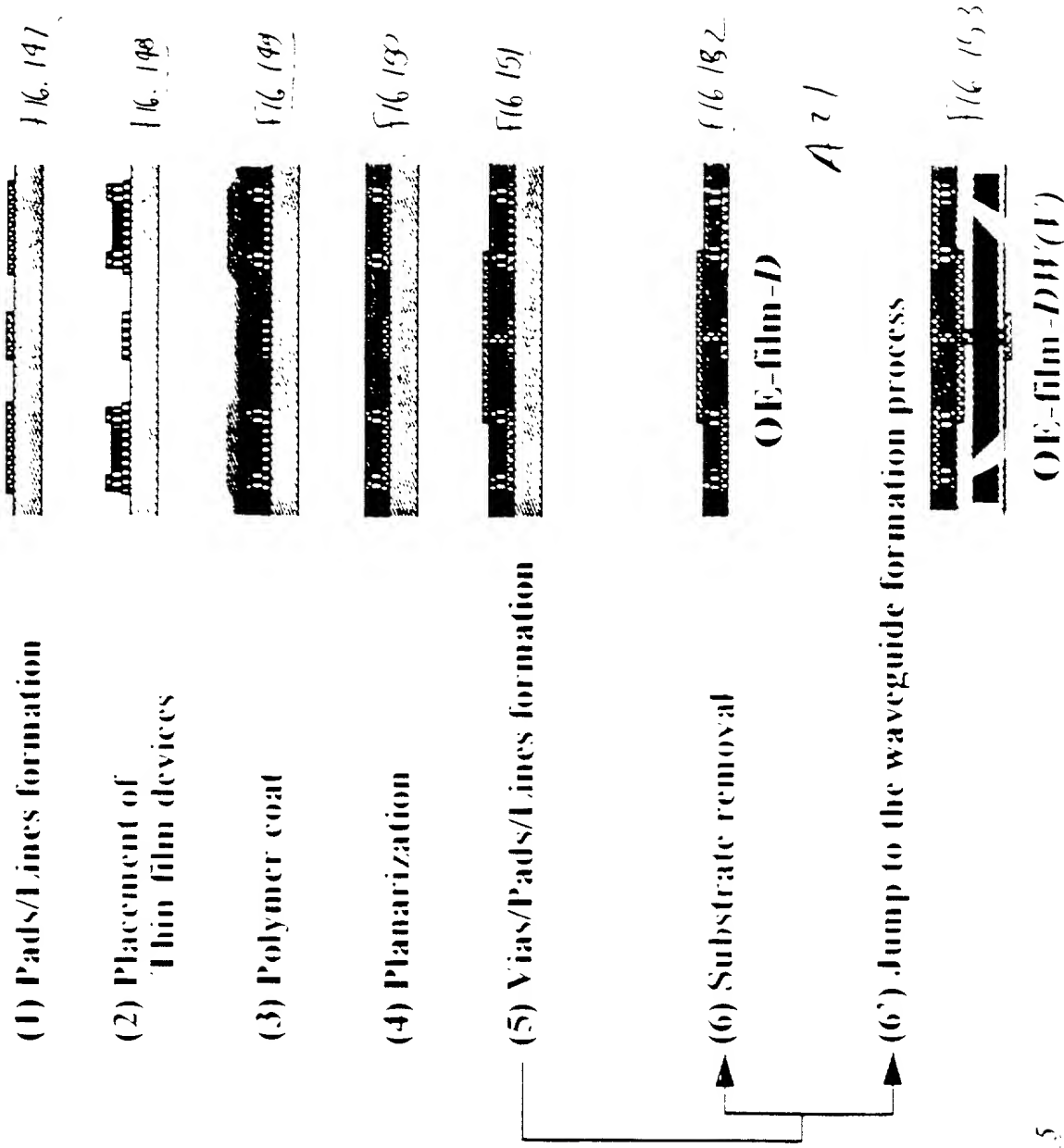


Fig. 3/19/99-1

Fig. 146

## Device Integration Process





1/XX

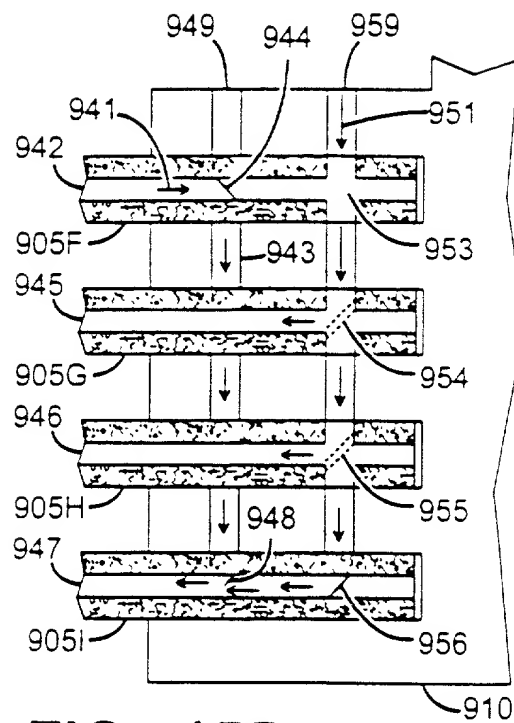


FIG. 155

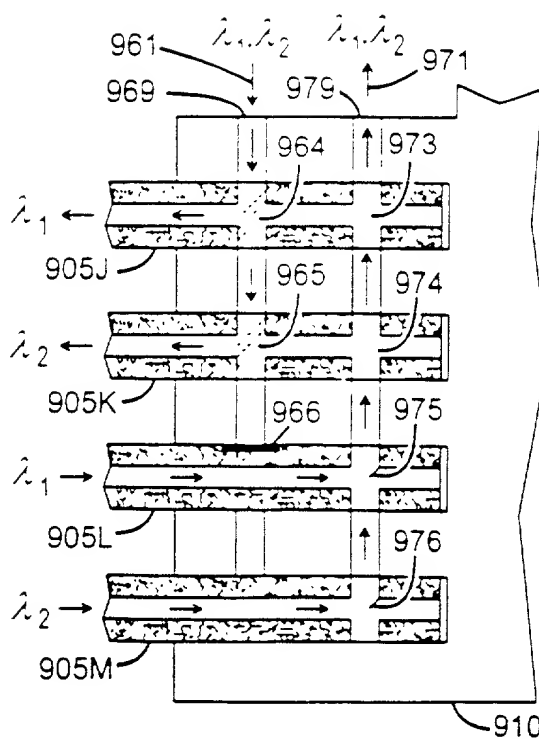


FIG. 156-1

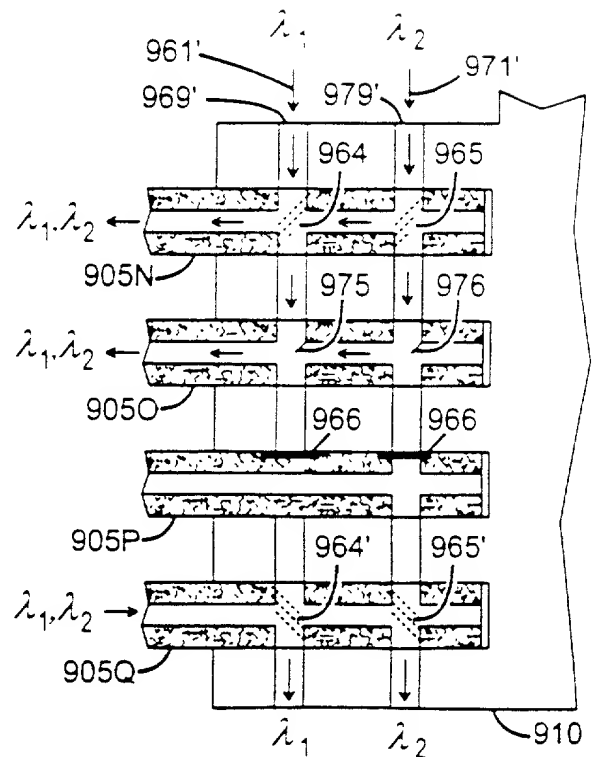


FIG. 156-2

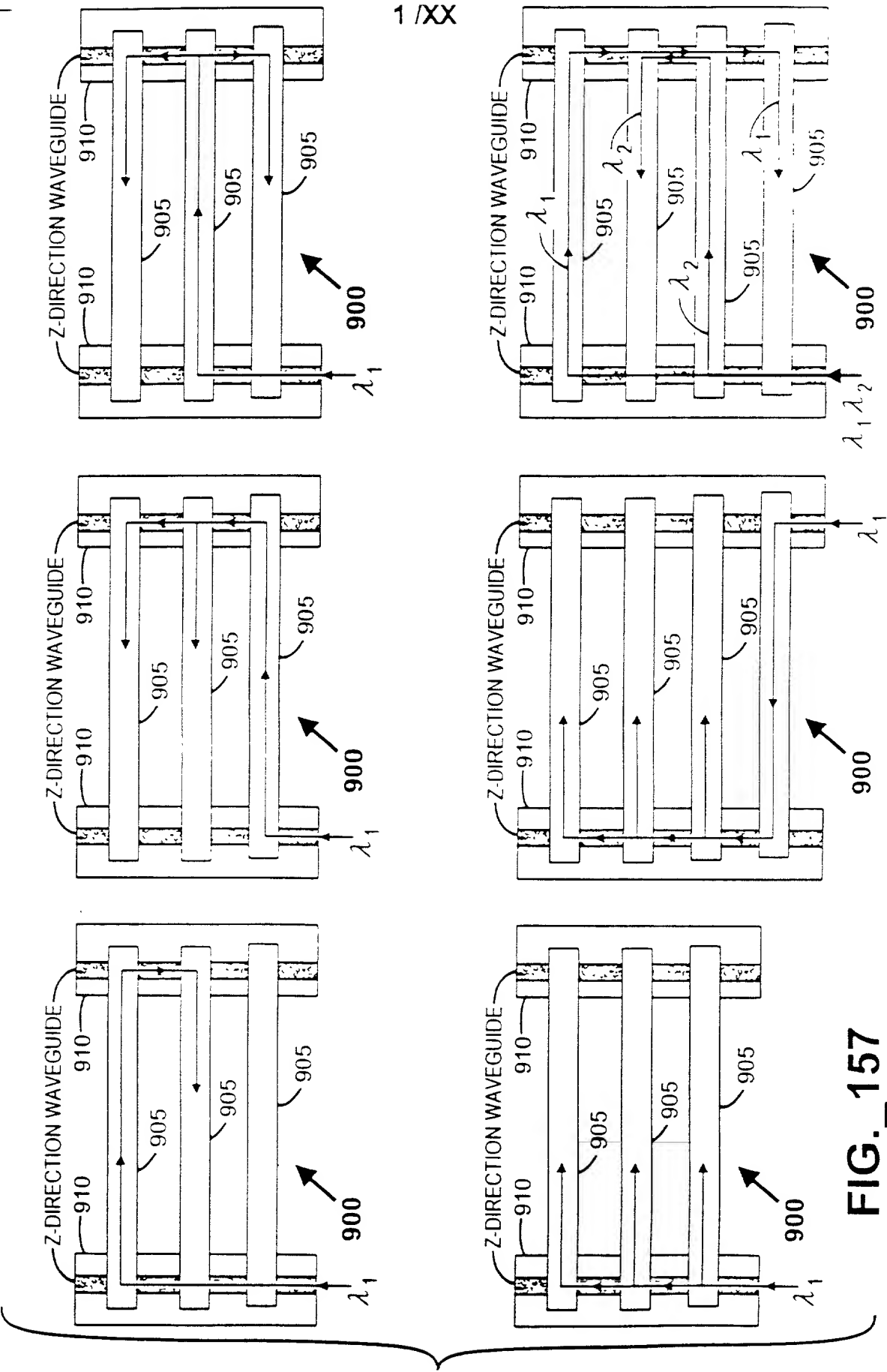


FIG. 157

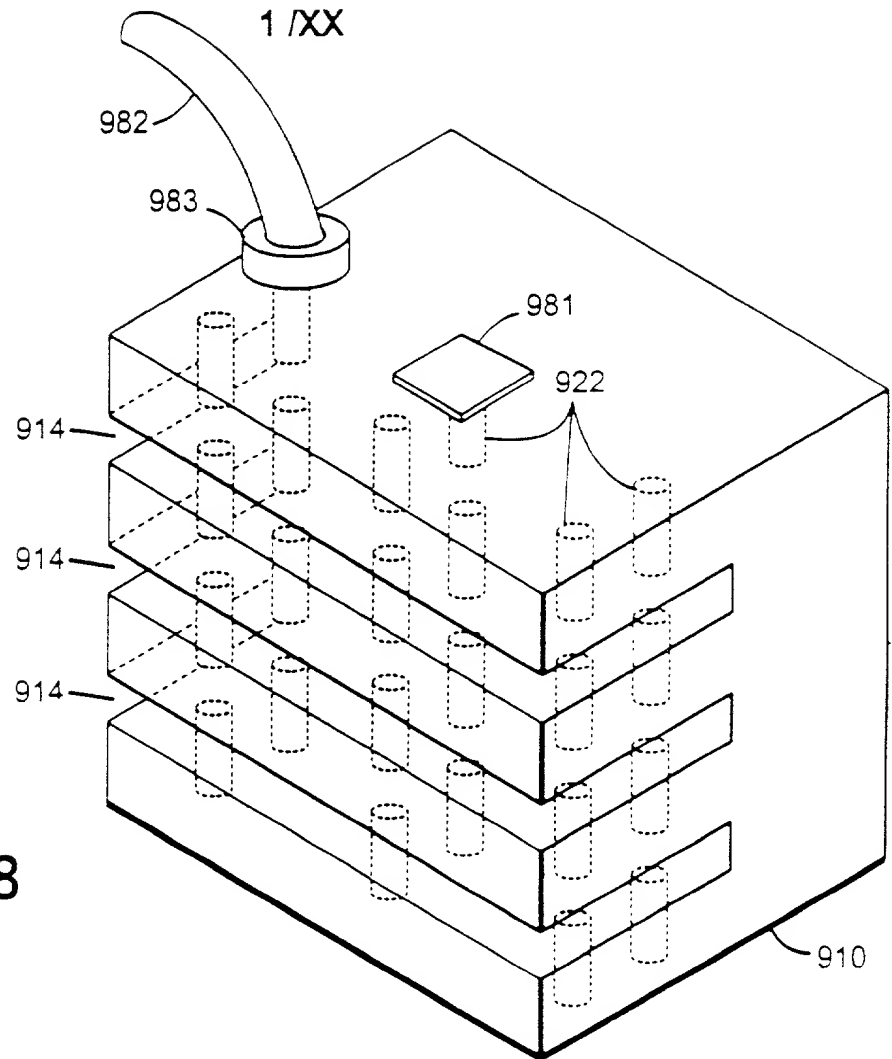


FIG.\_158

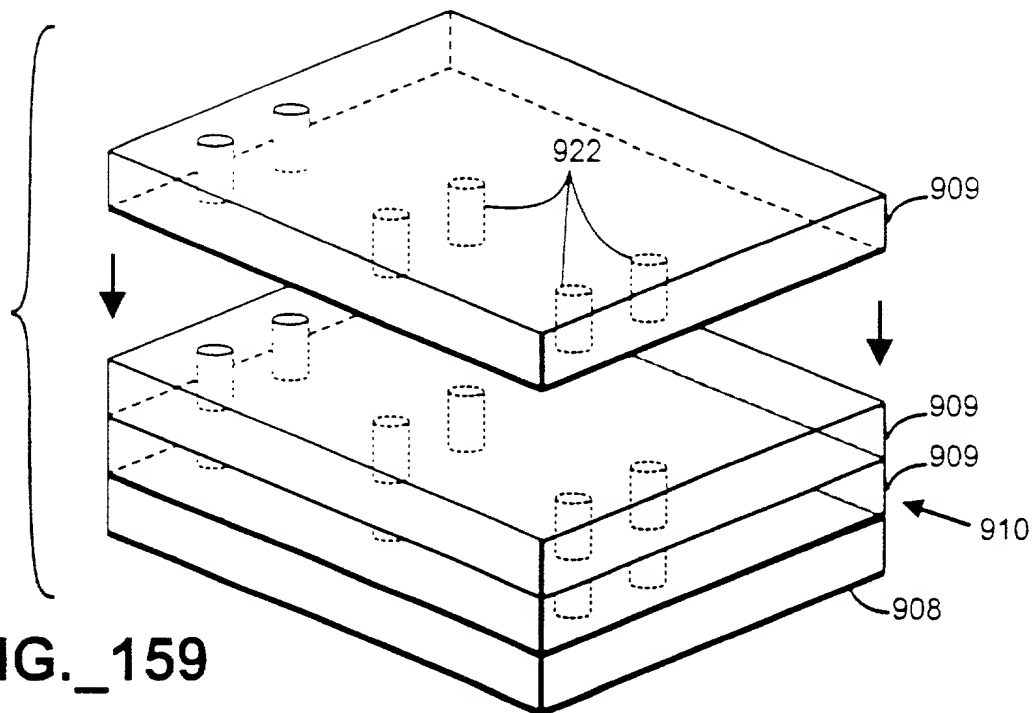


FIG.\_159

FIG.\_160

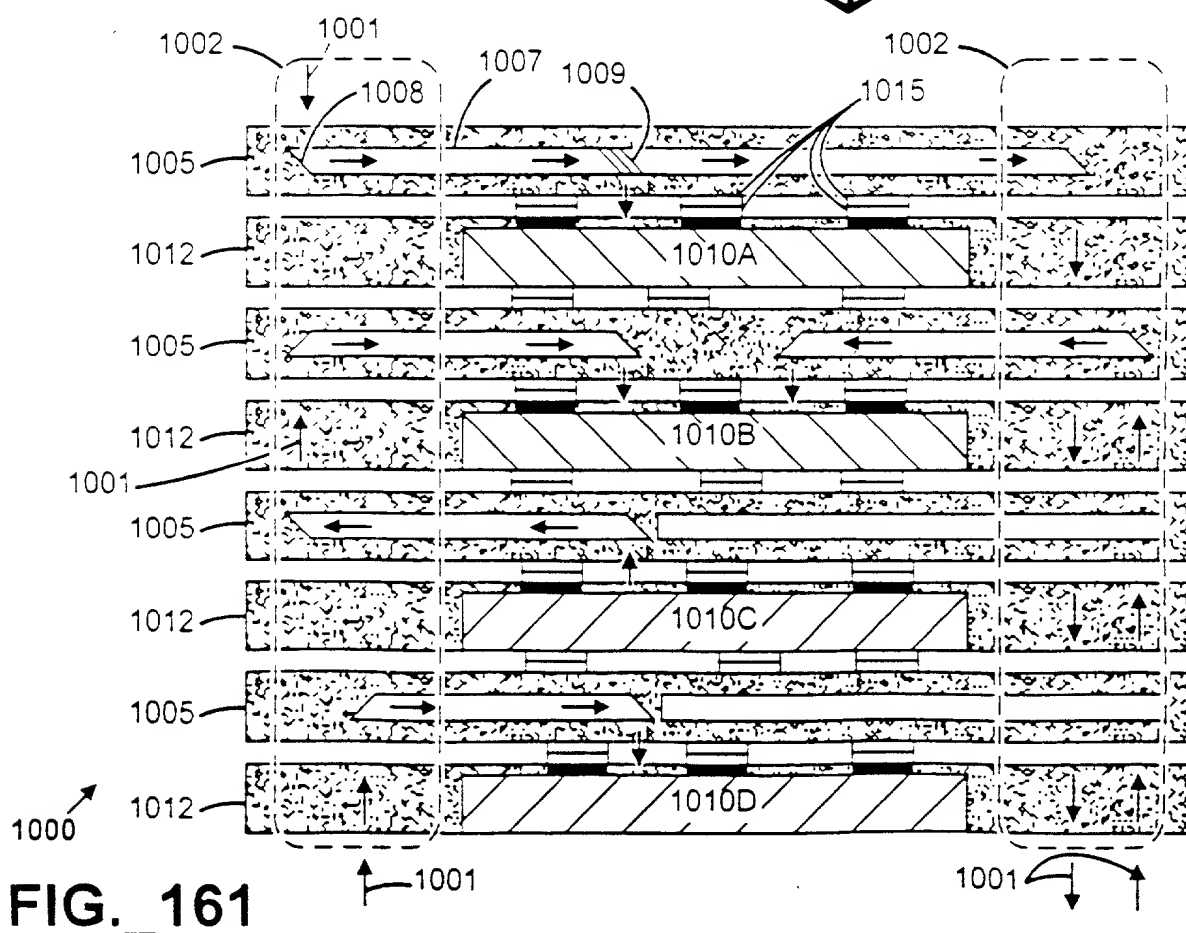
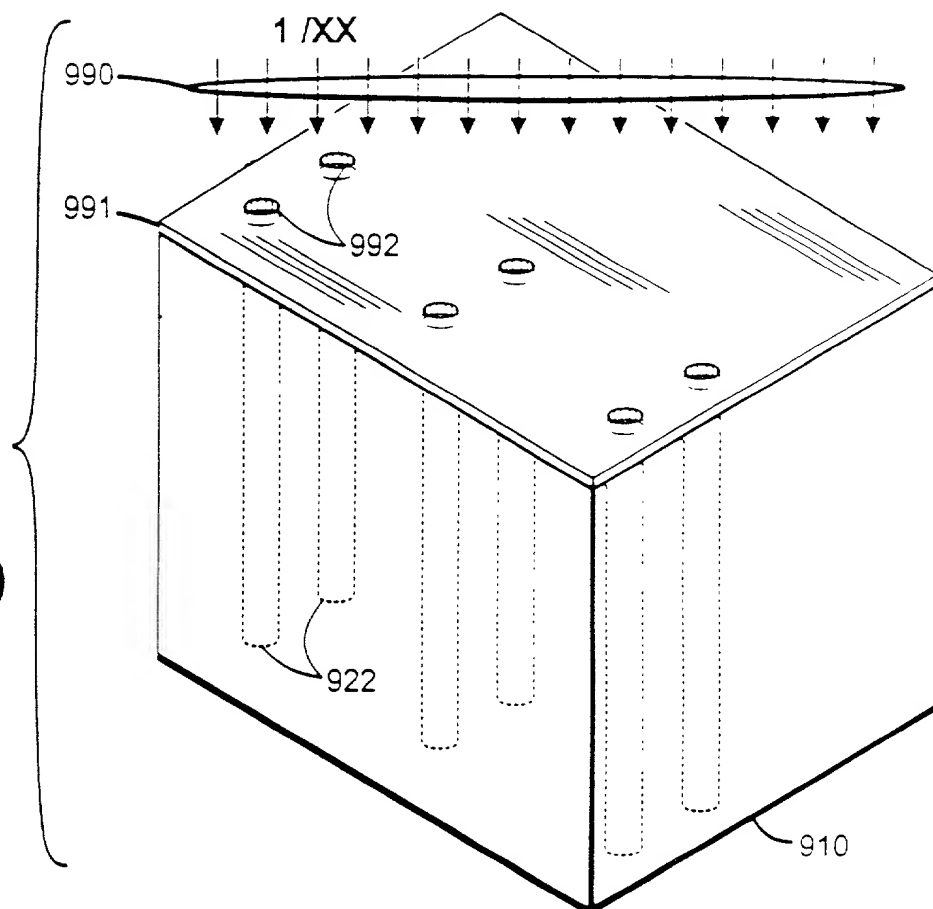
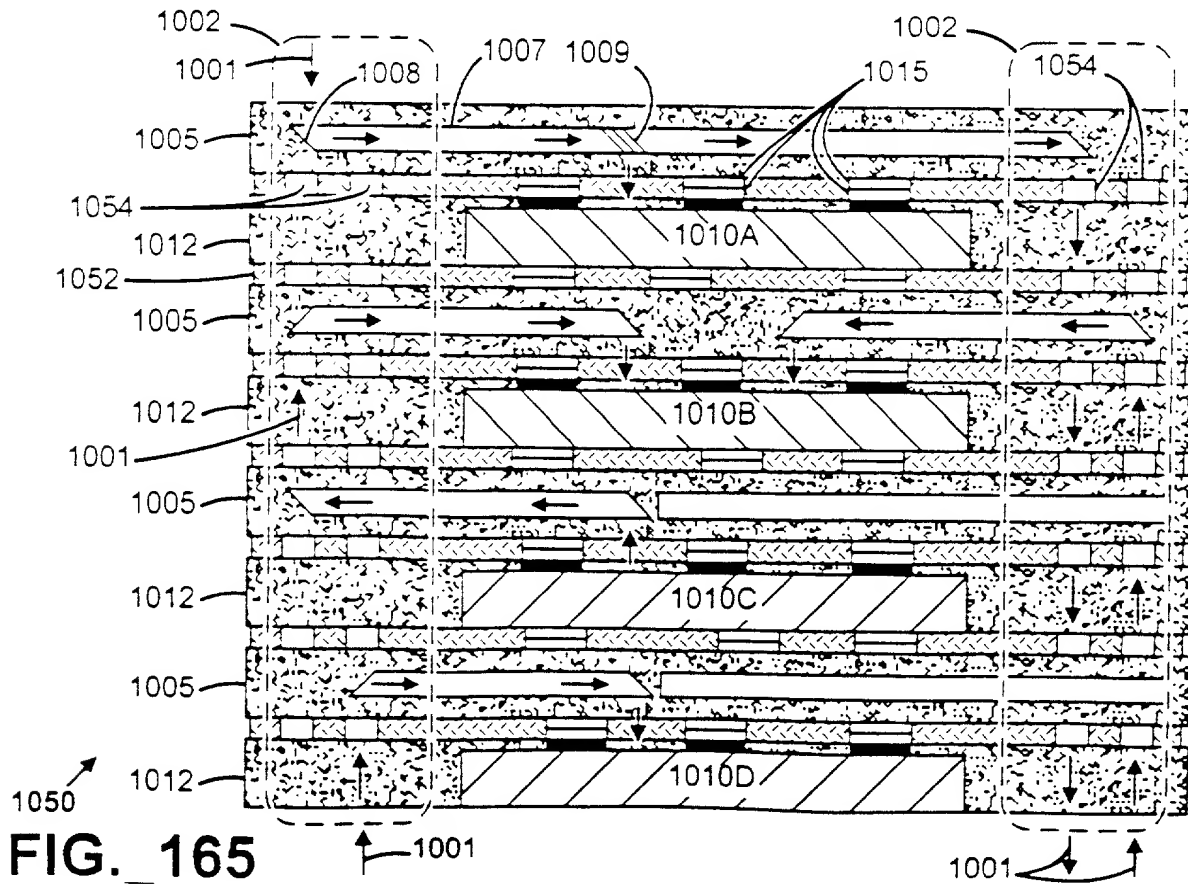
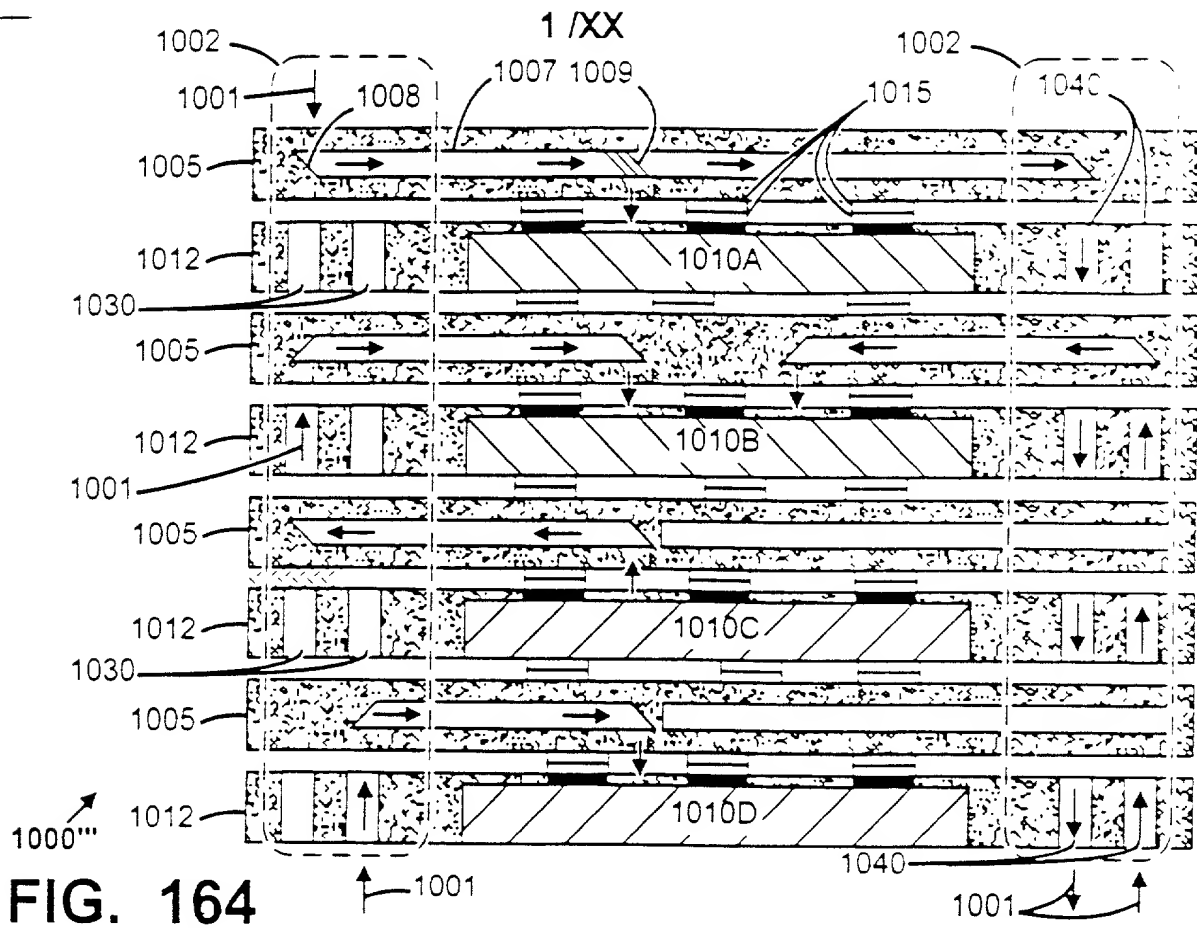


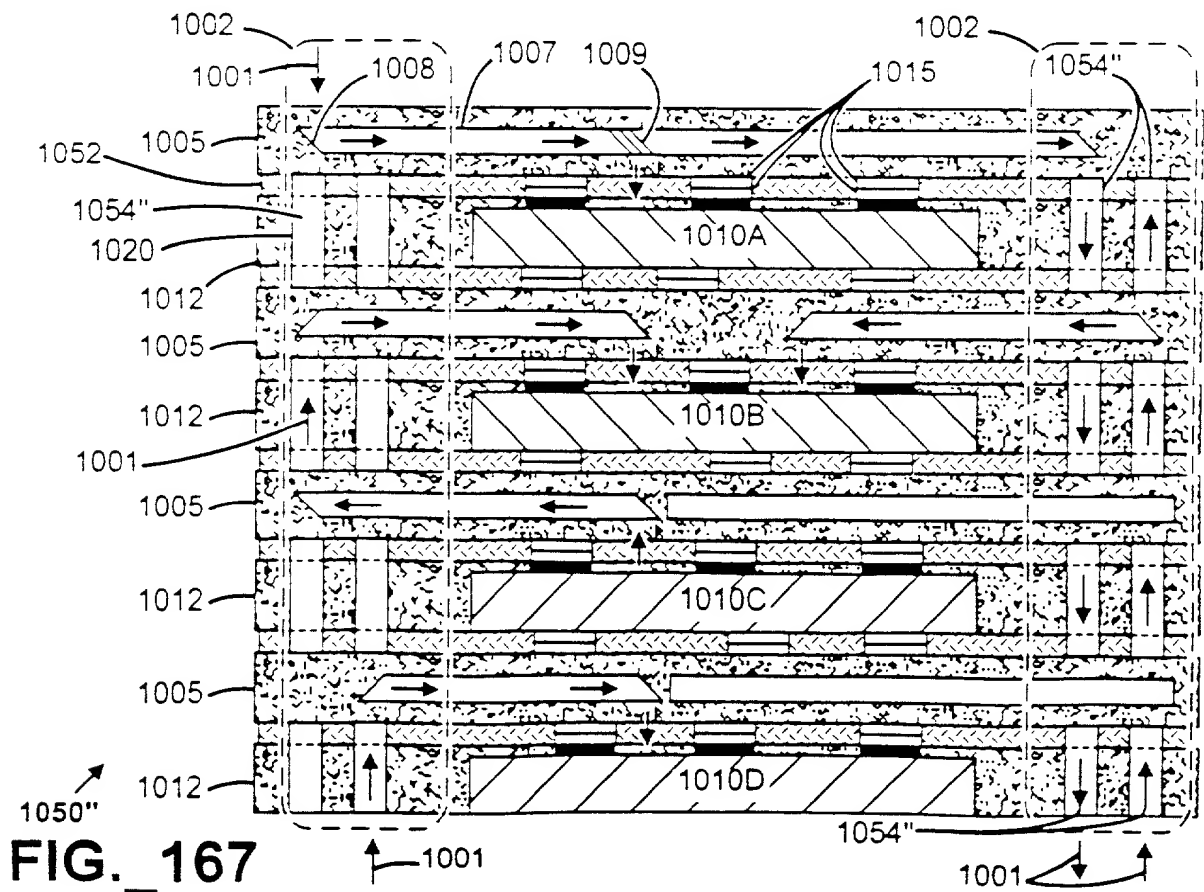
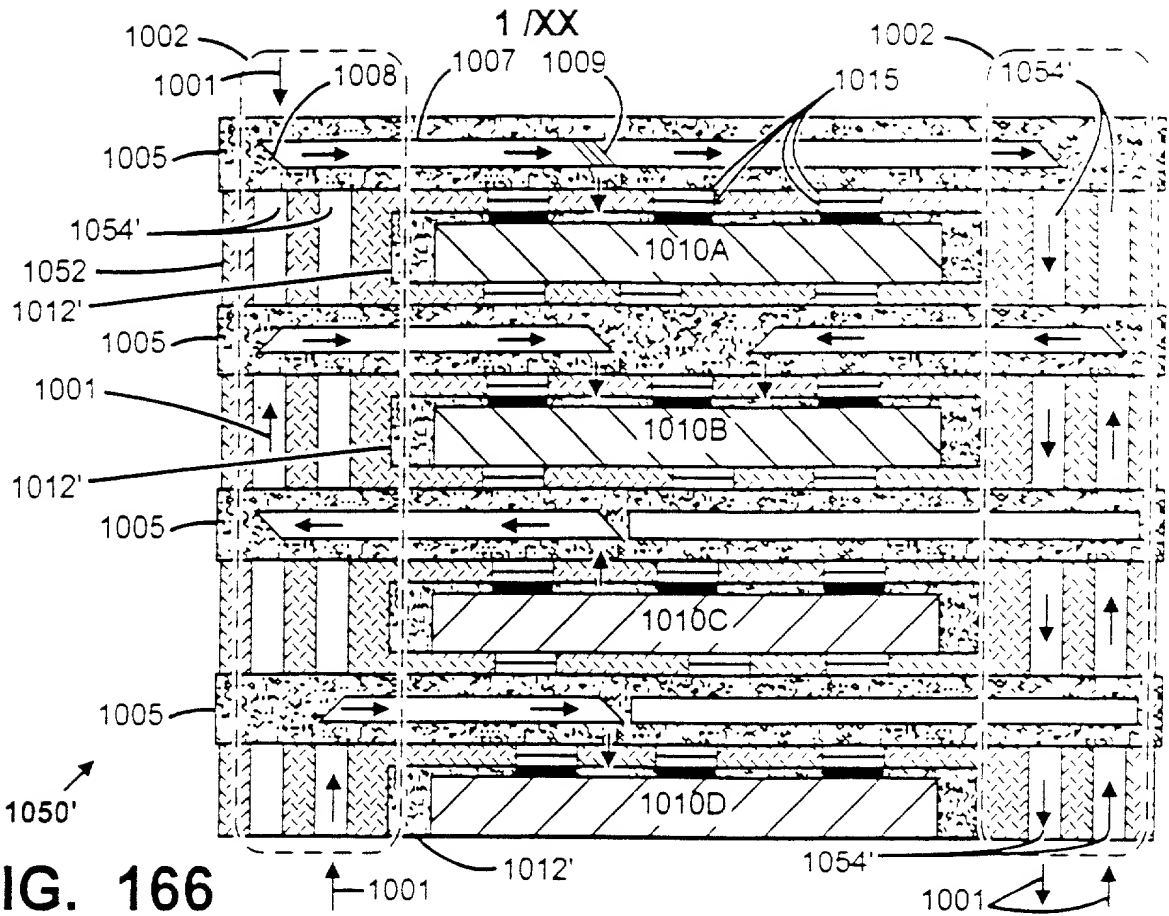
FIG.\_161







102210" 28529460





1/XX

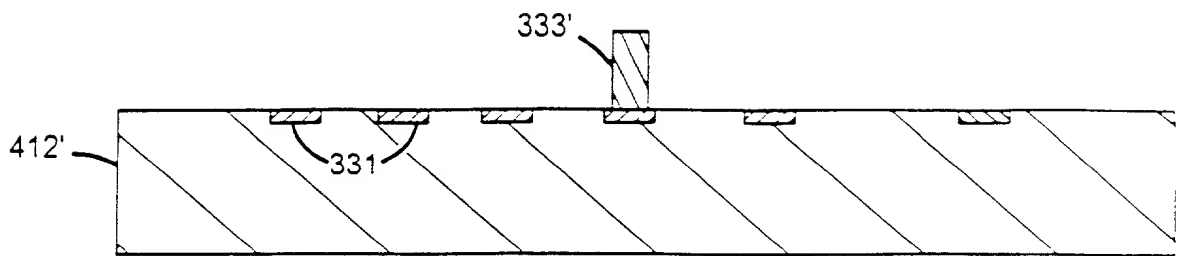


FIG.\_170

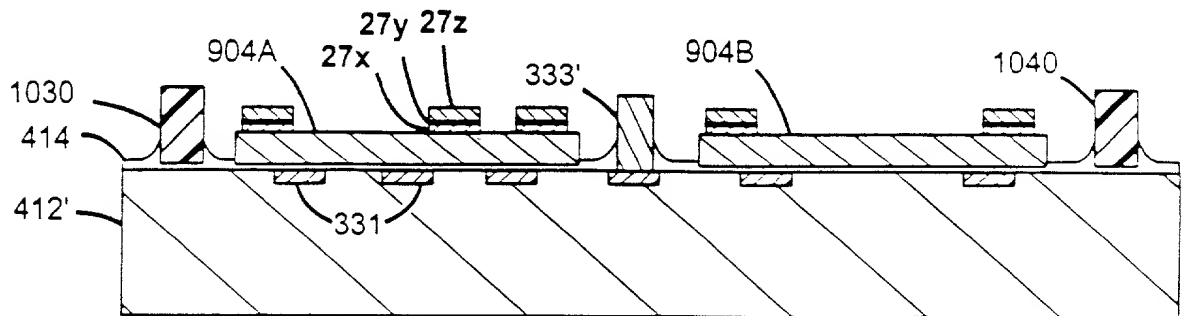


FIG.\_171

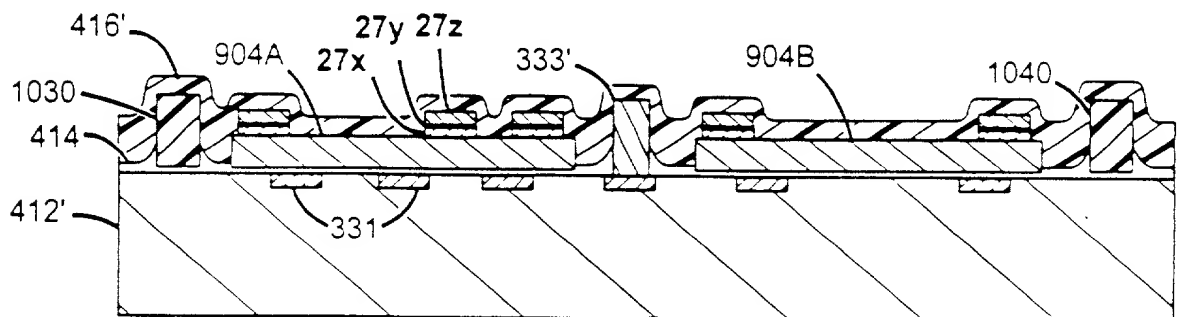


FIG.\_172

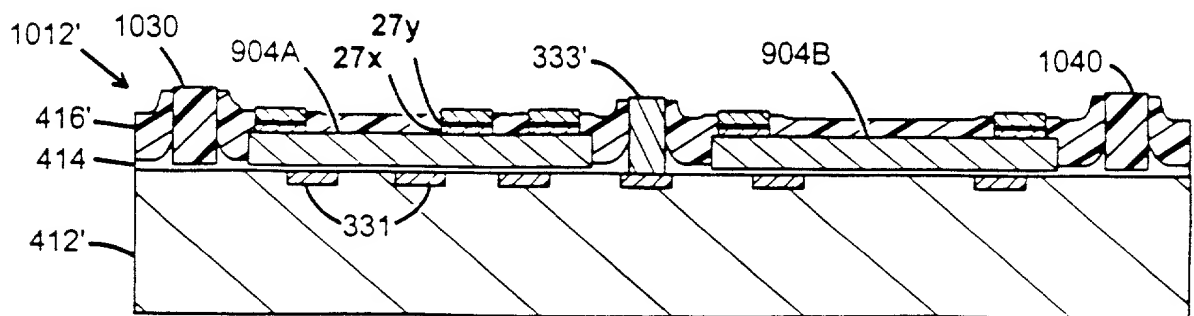


FIG.\_173

1 /XX

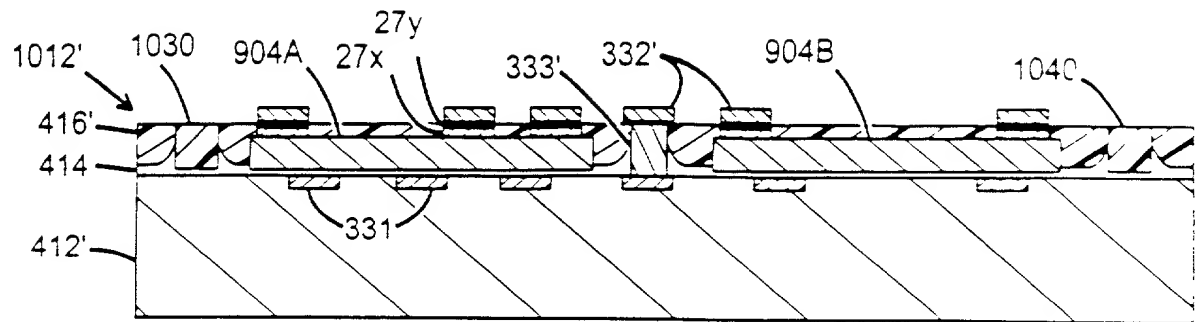


FIG.\_174

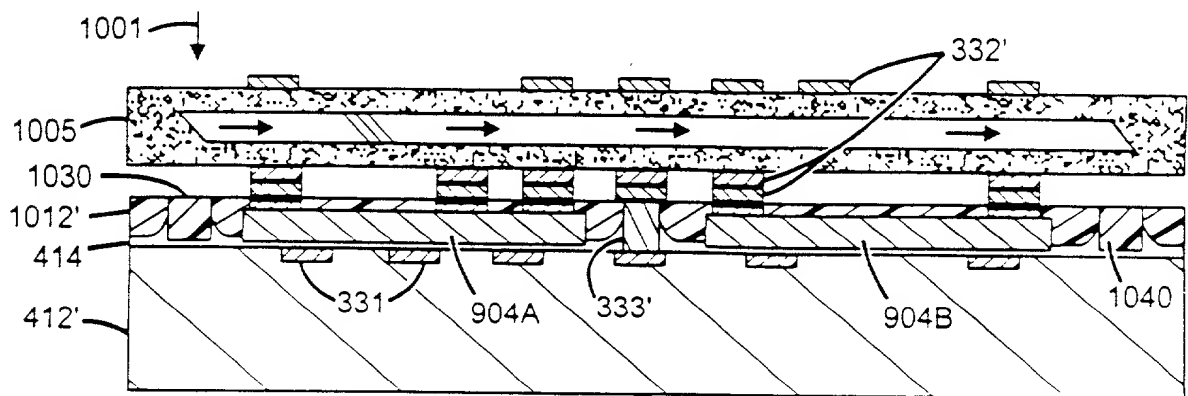


FIG.\_175

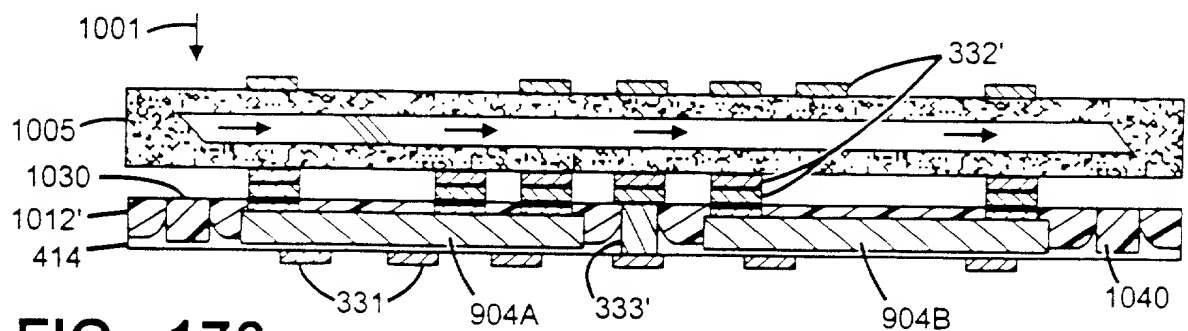


FIG.\_176

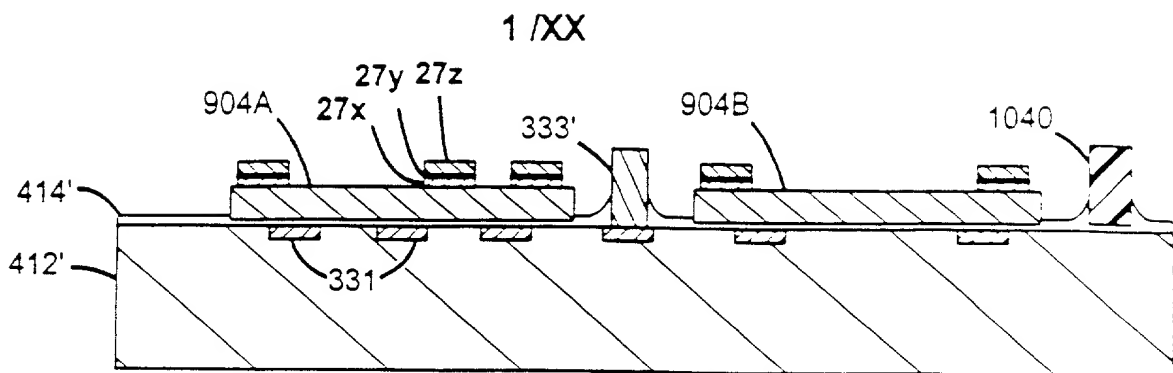


FIG.\_177

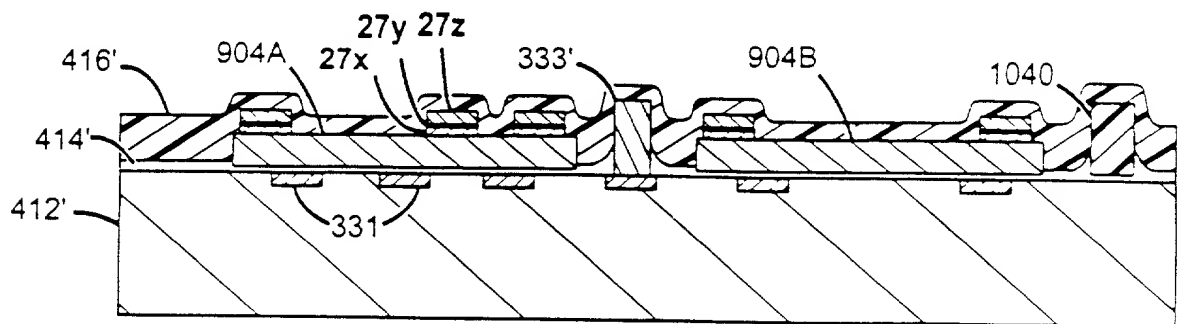


FIG.\_178

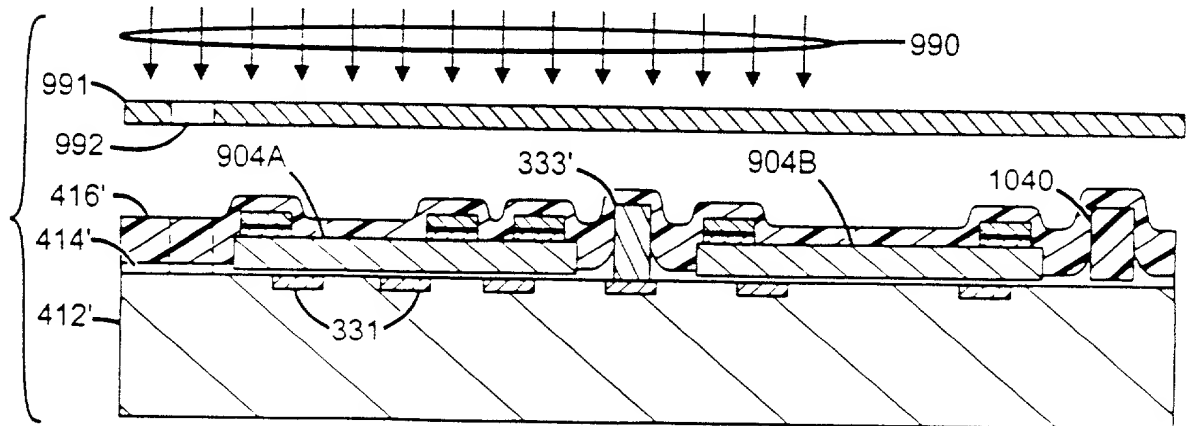


FIG.\_179

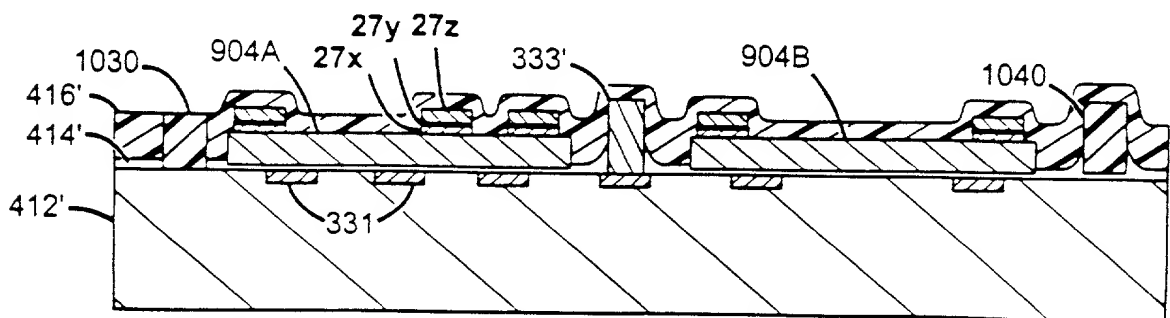
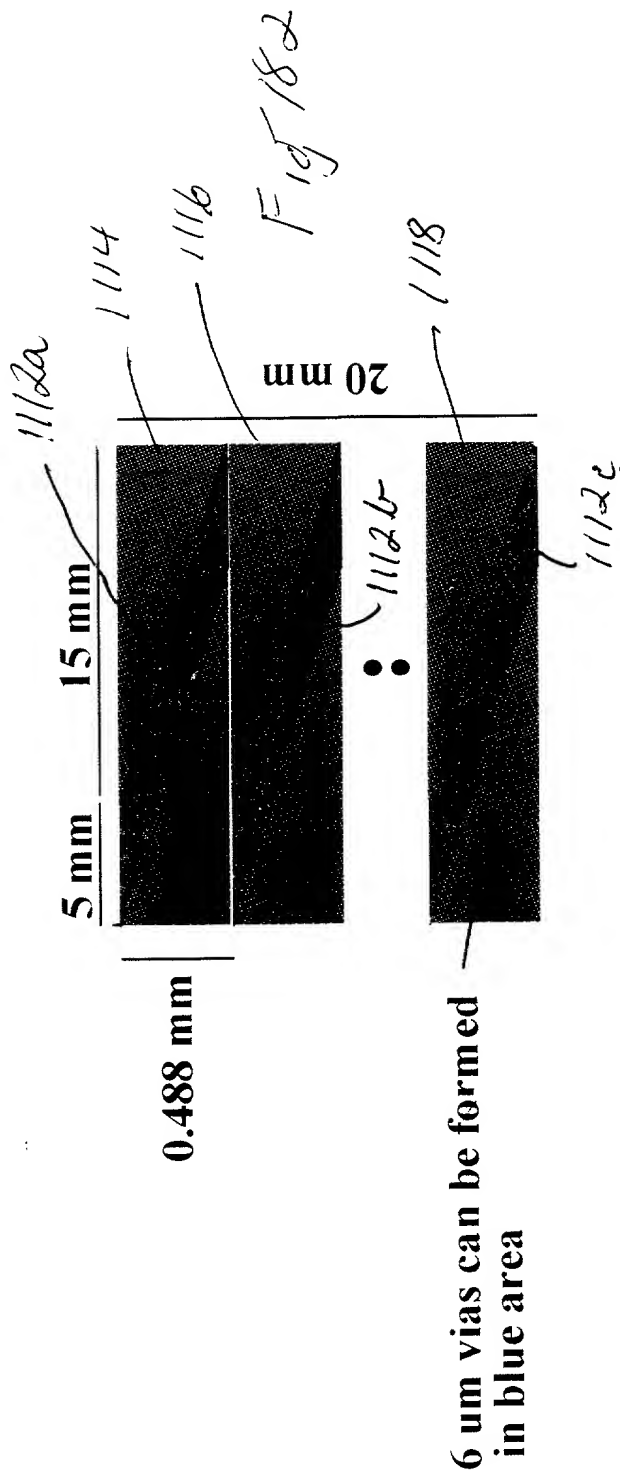
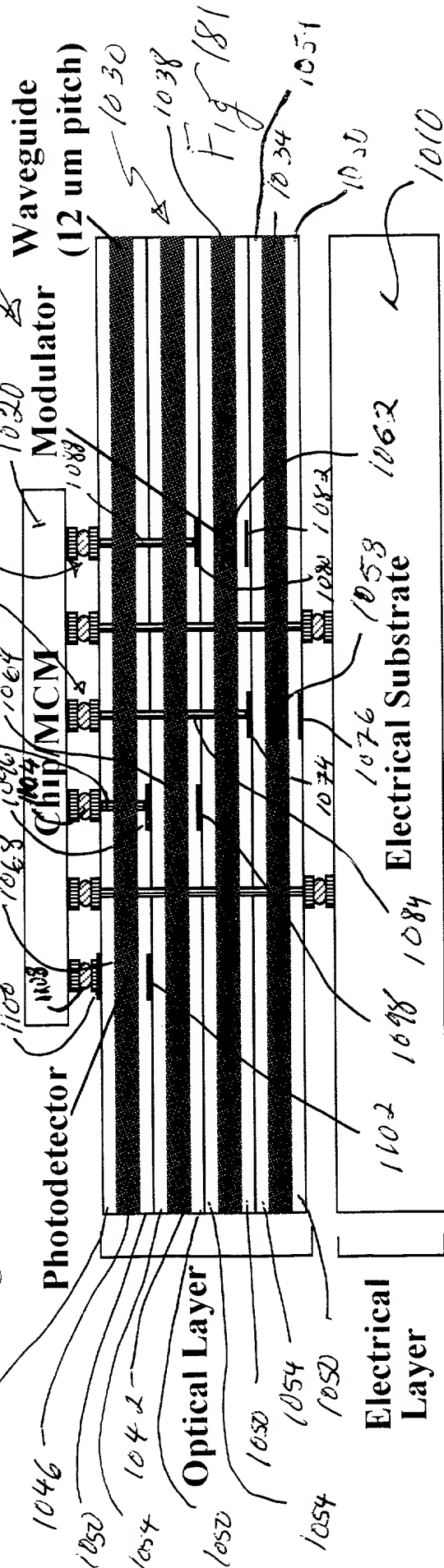


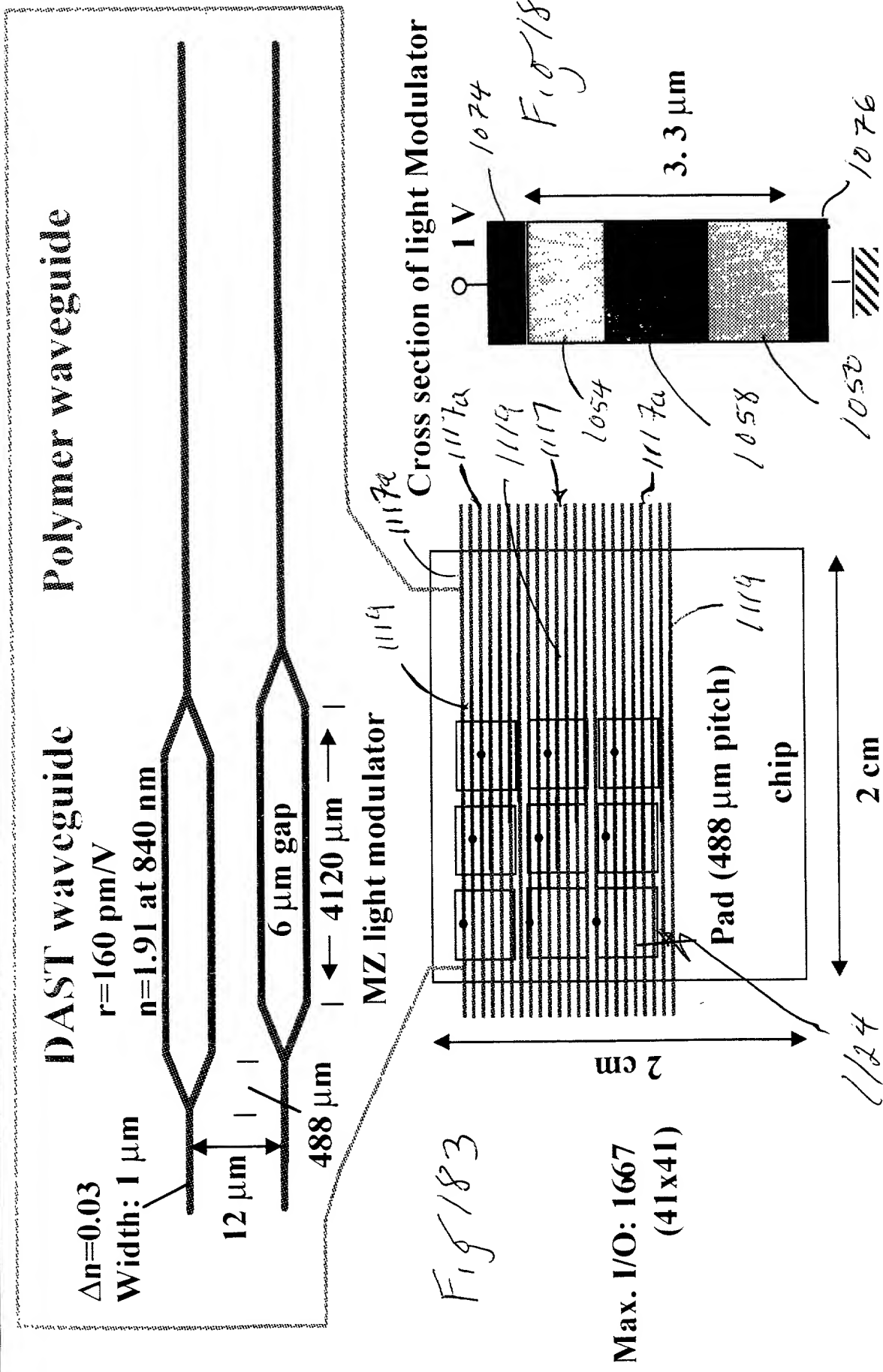
FIG.\_180

# I/O Connection in OE Substrate (Planar Modulator)

**Signal I/O count:  $6000 = \lfloor 1500 \text{ I/O per Layer} \rfloor \times \lfloor 4\text{-Layer} \rfloor$**



# I/O Connection in OE Substrate (Planar Modulator)



Max. I/O: 1667  
(41x41)



# I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

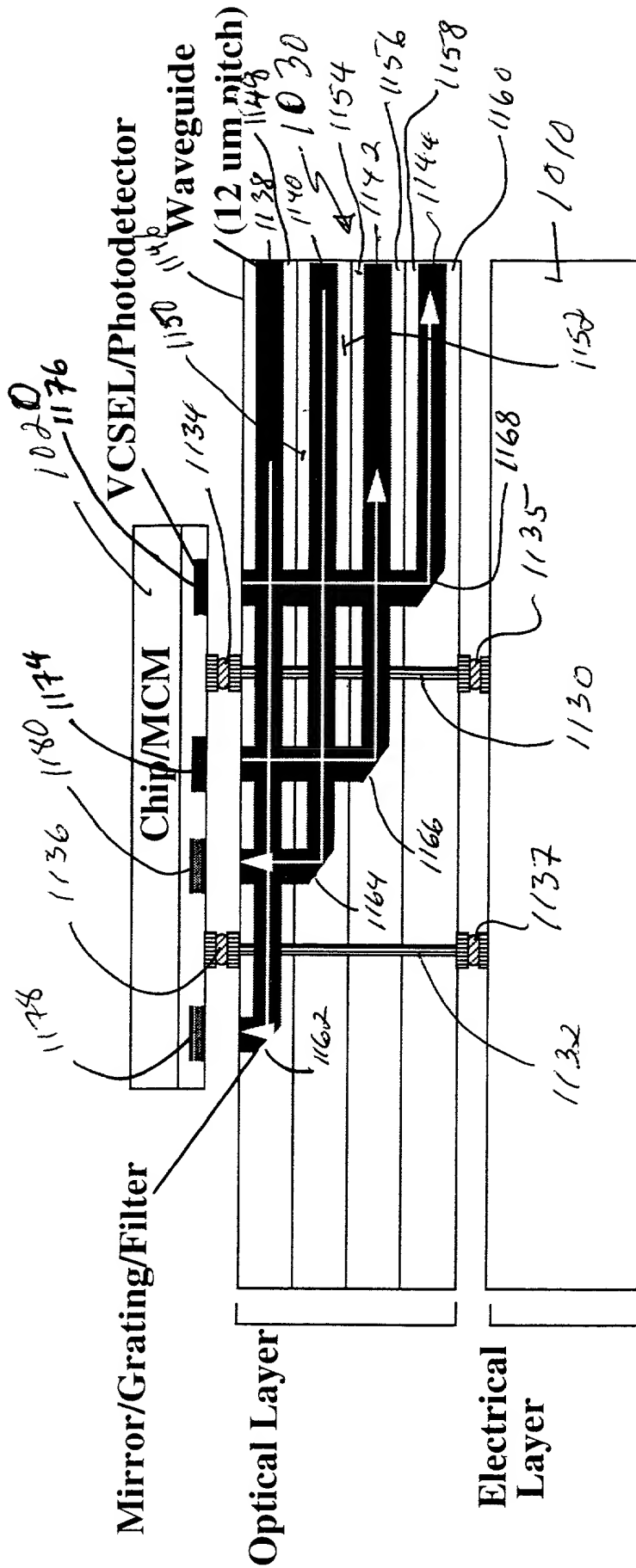
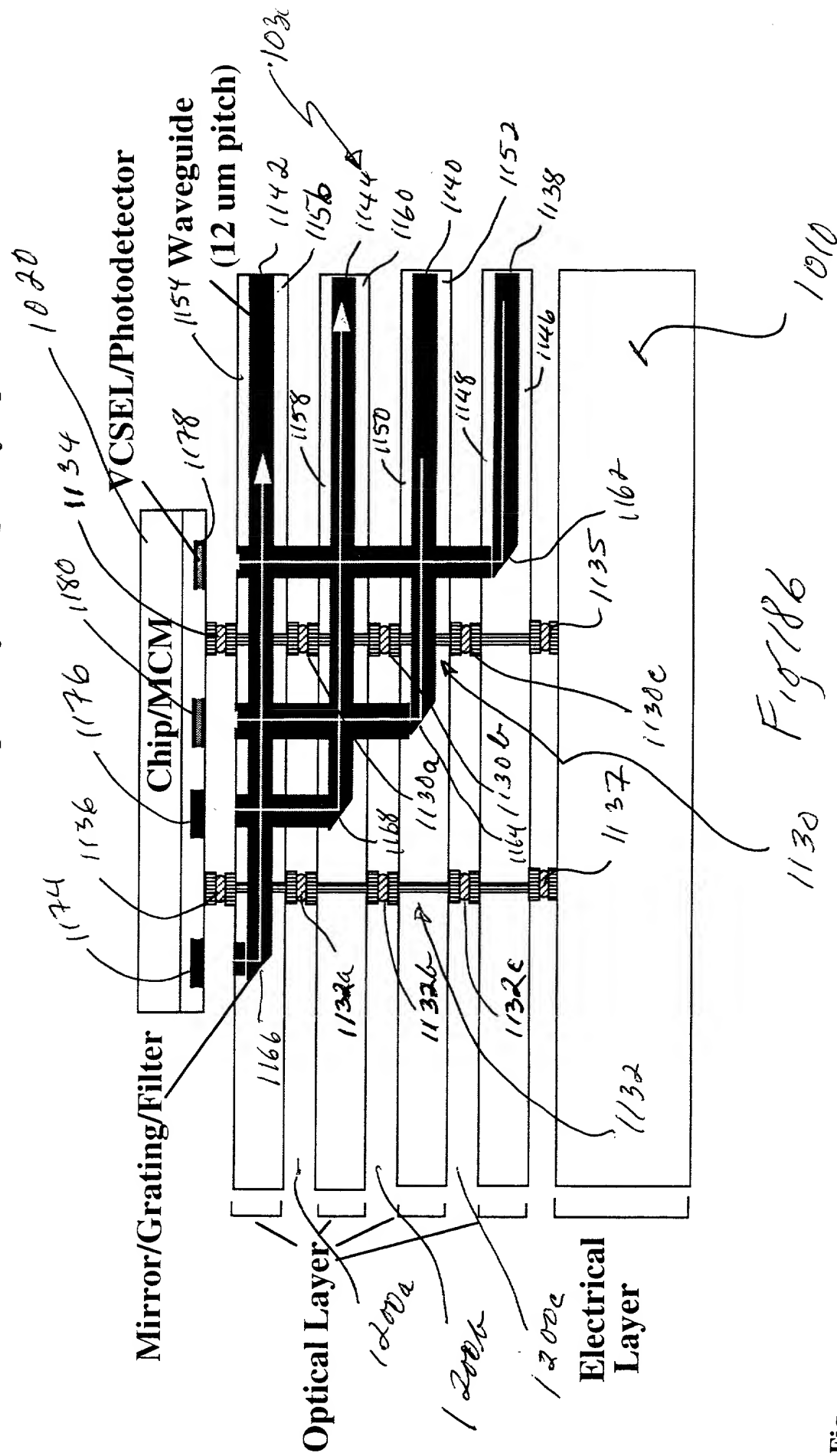


Fig 185

# I/O Connection in OE Substrate (OE-VLSI)

**Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]**

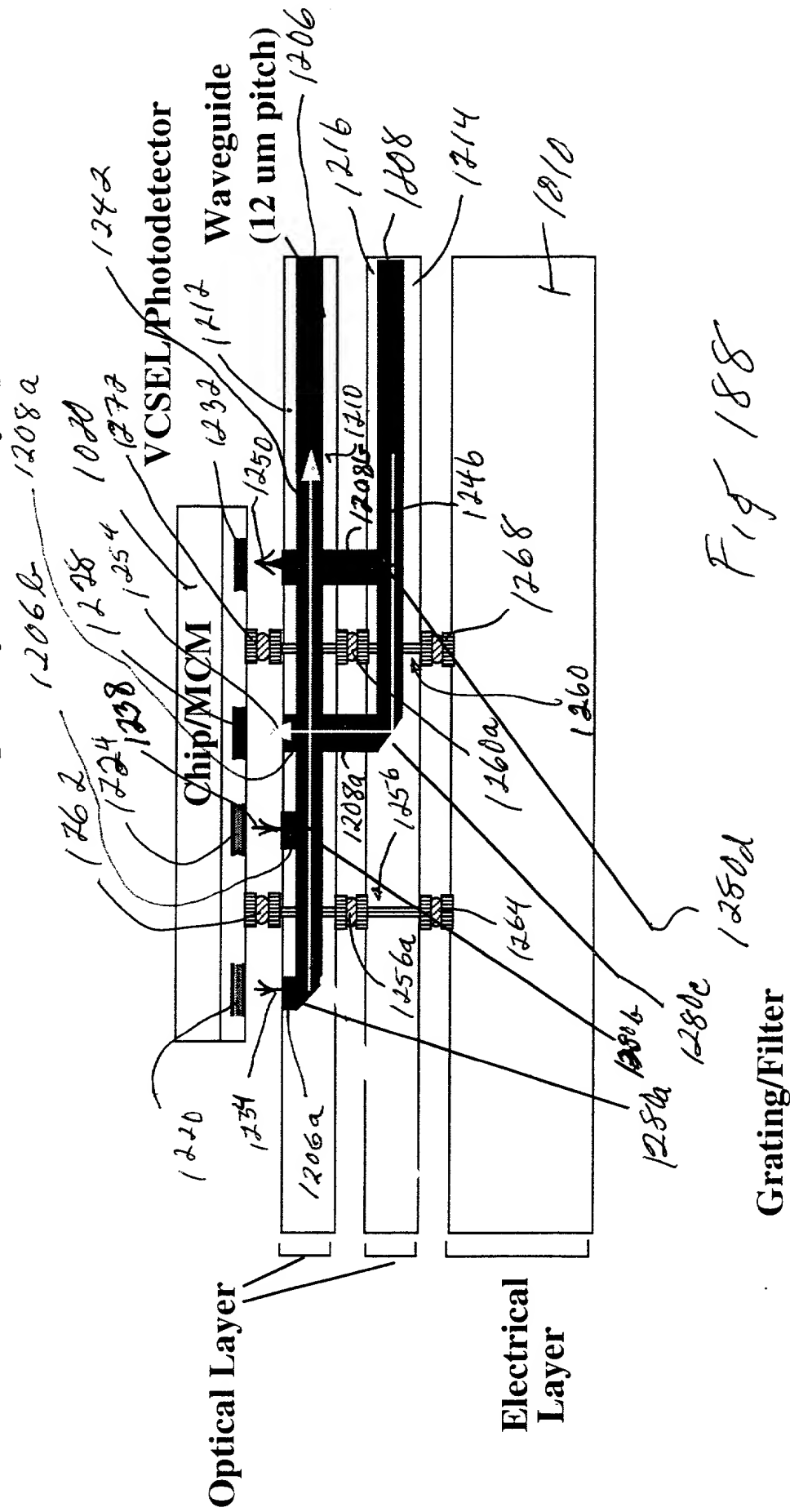


**Fig.**



# I/O Connection in OE Substrate (OE-VLSI, WDM)

**Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]**



F, 188

# Grating/Filter

# I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

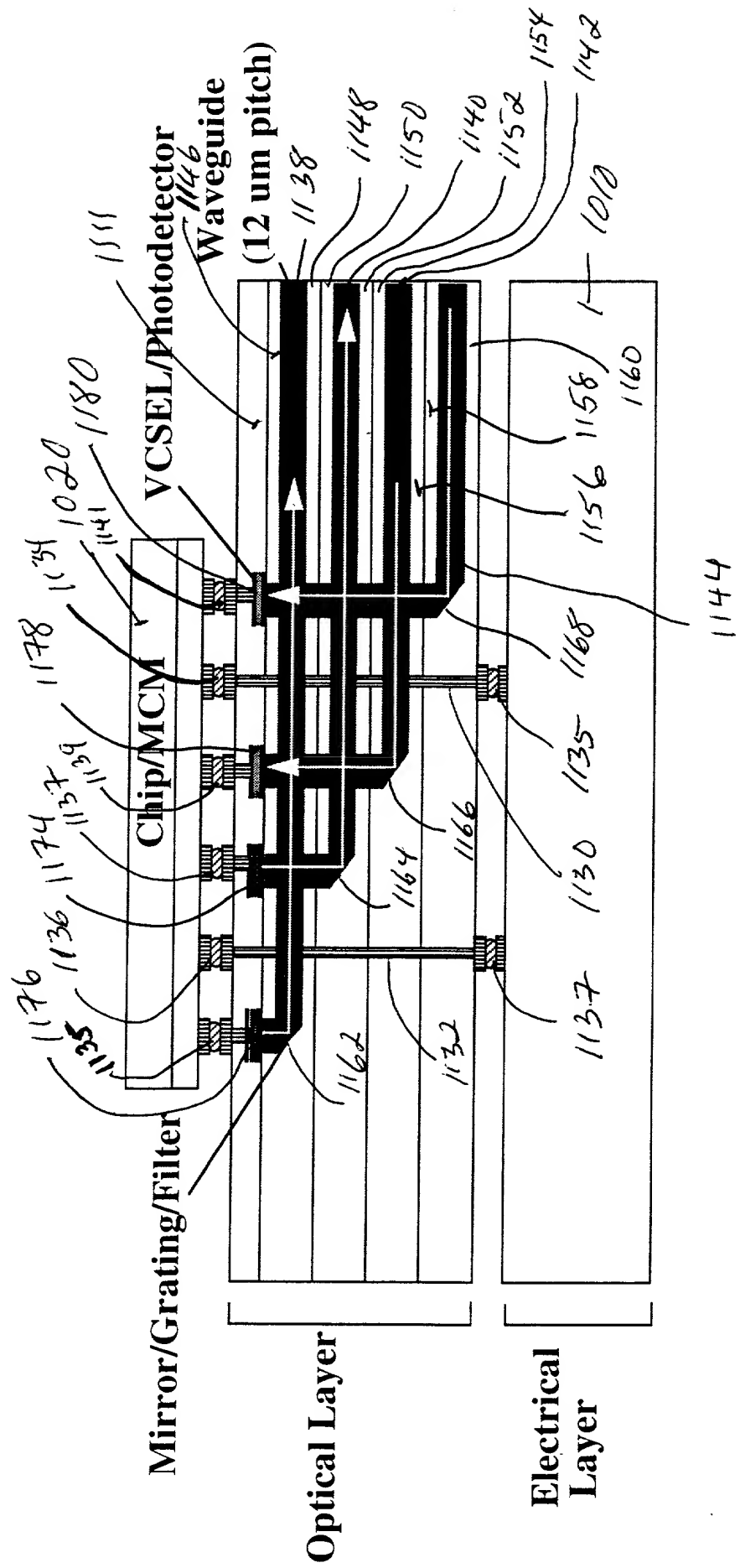


Fig 189

# I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

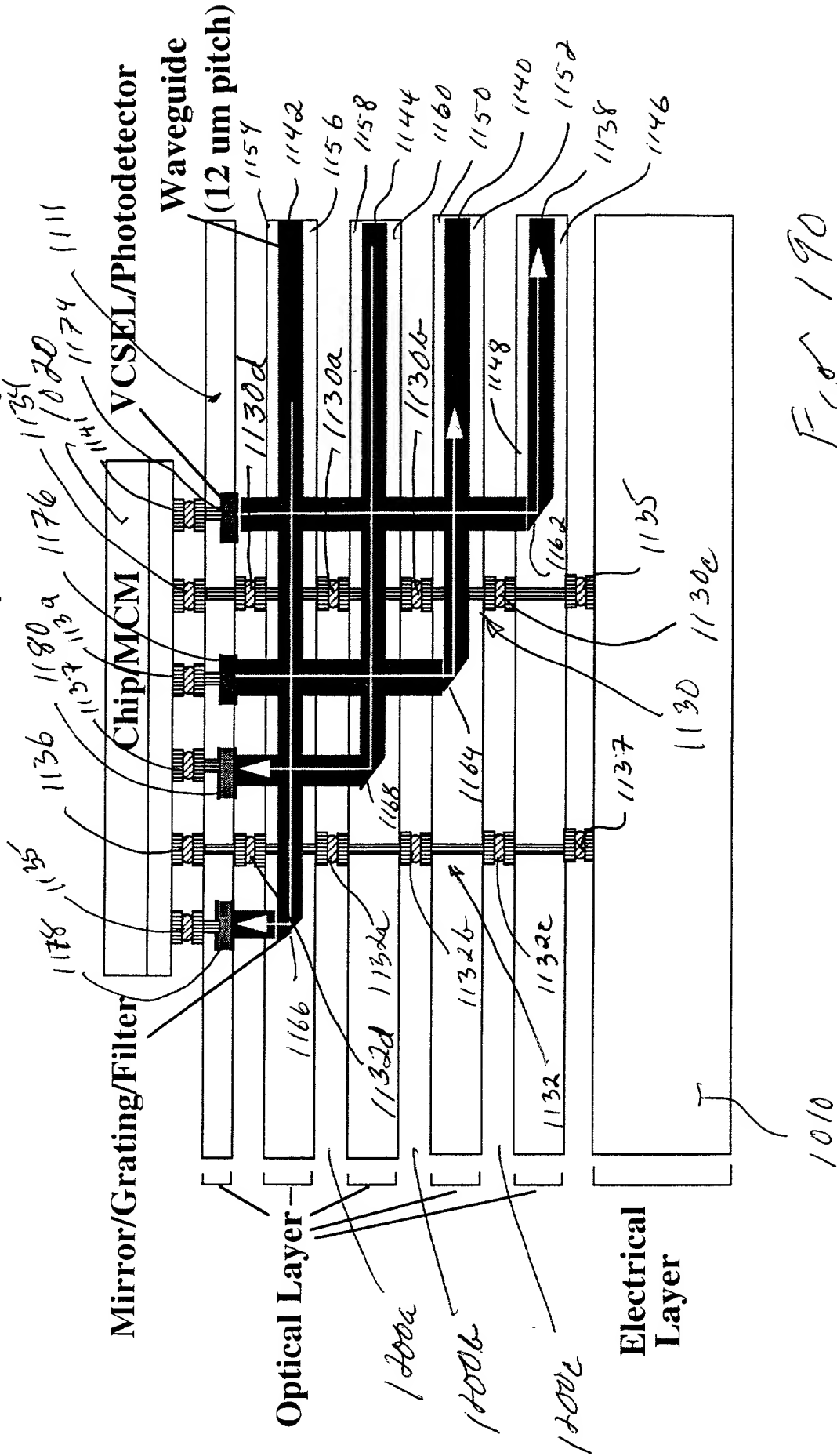


Fig. 9

Fig 190

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (Active OE Layer, WDM)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

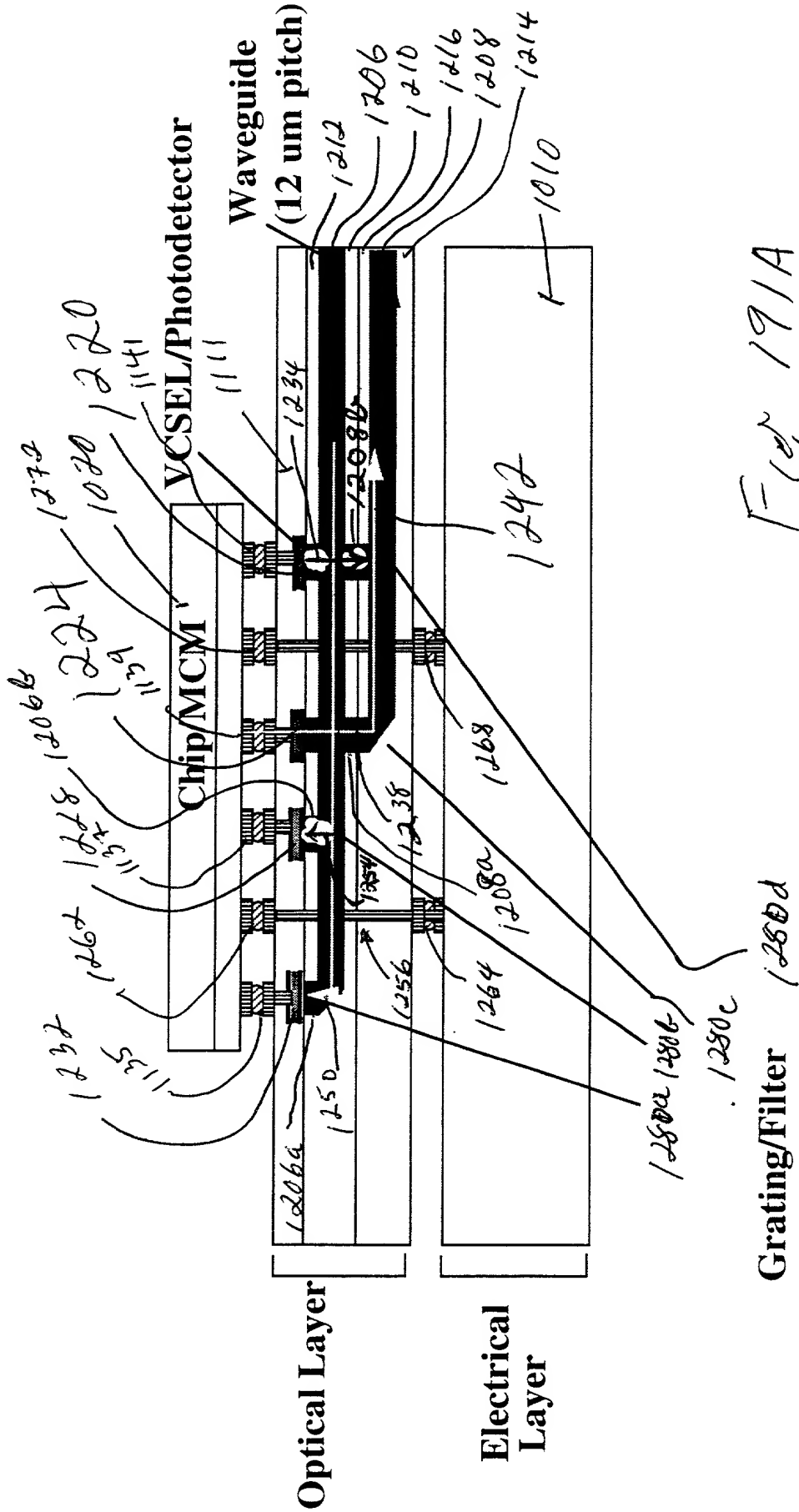


Fig. 10

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (Active OE Layer, WDM)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

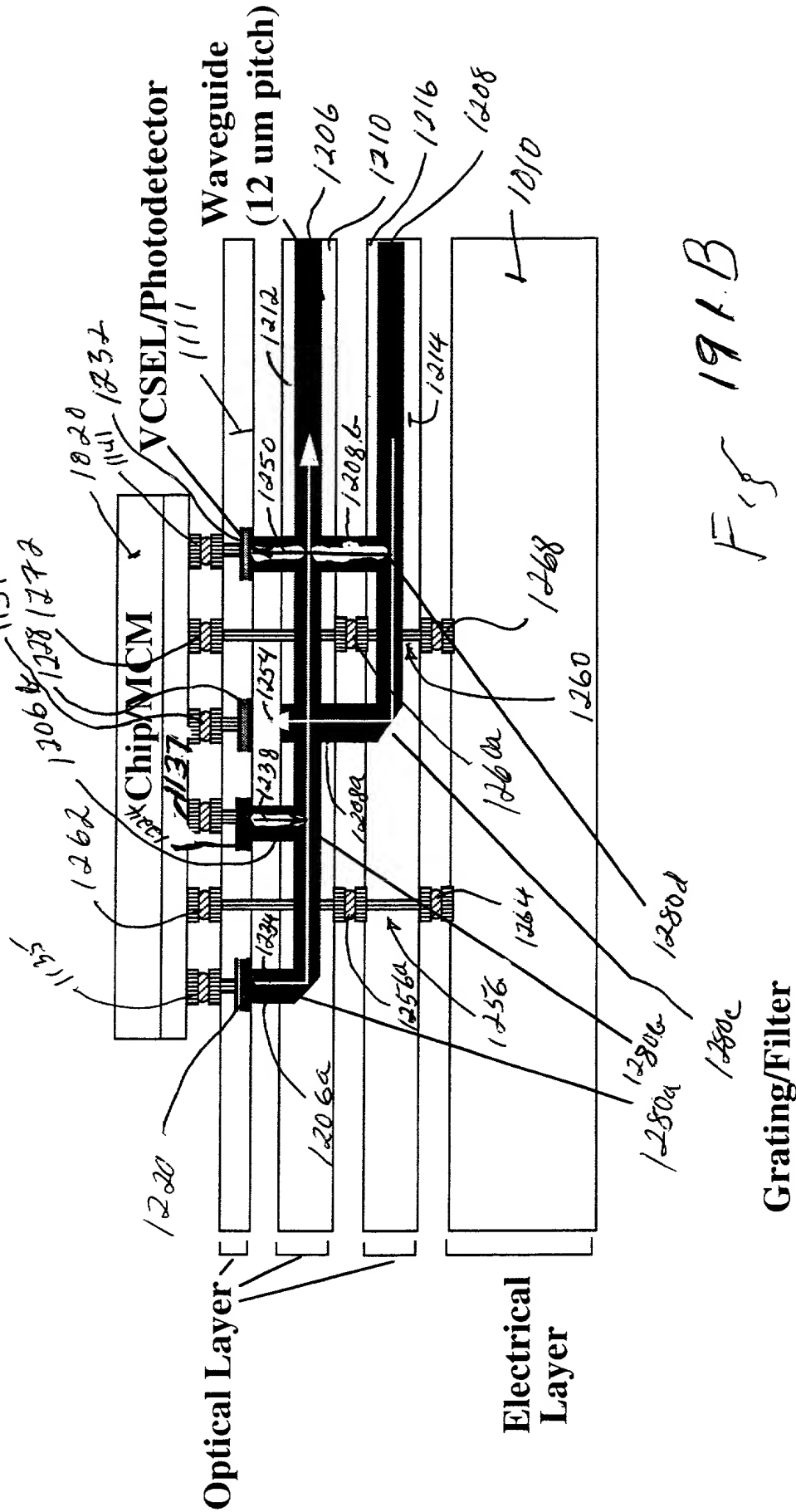
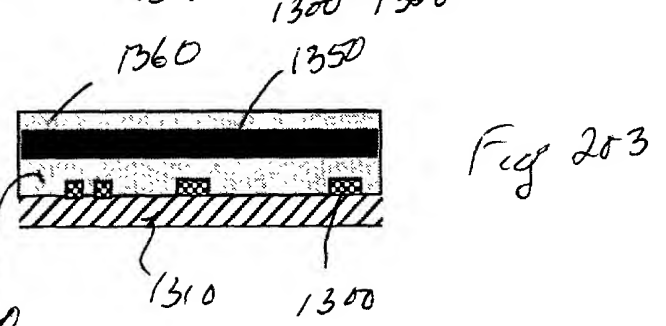
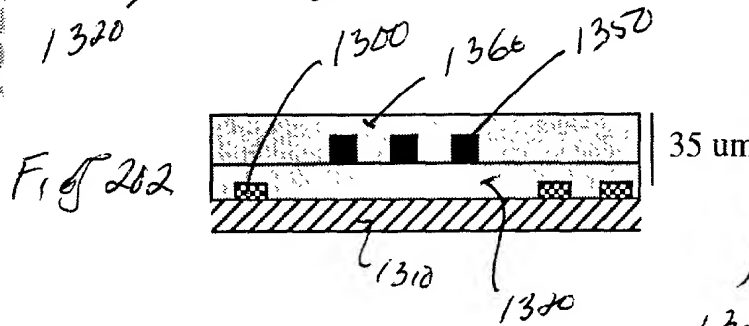
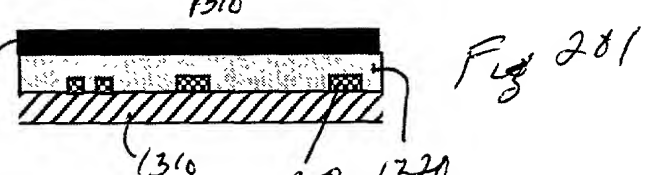
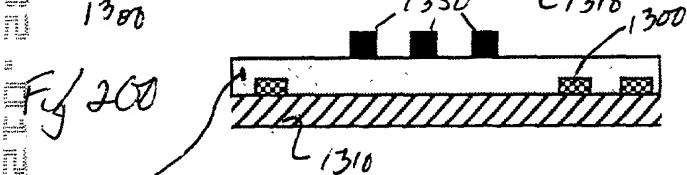
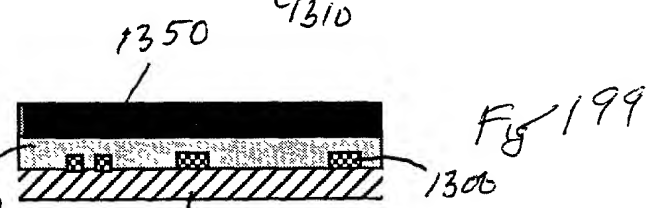
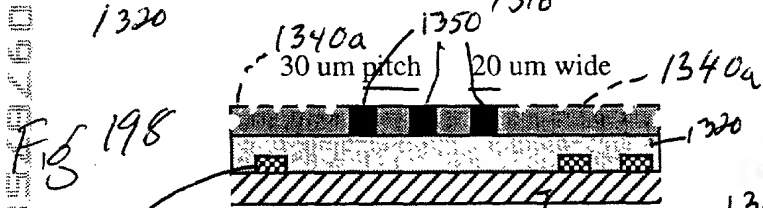
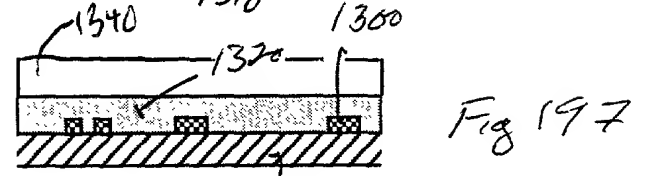
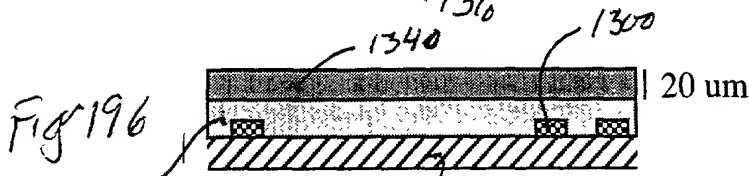
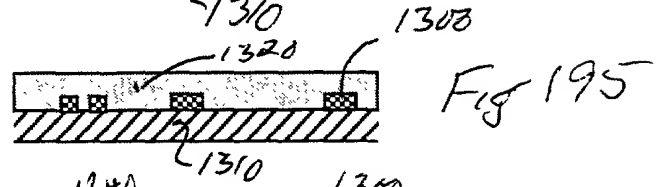
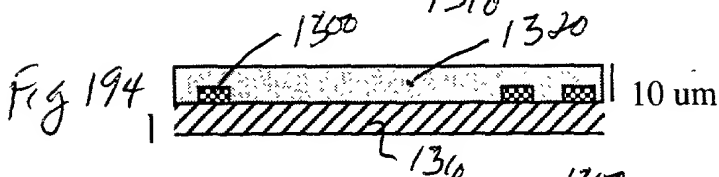
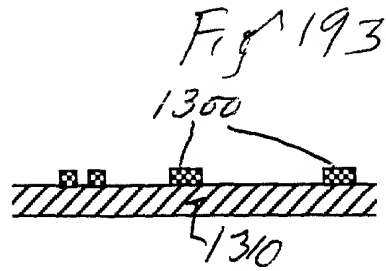
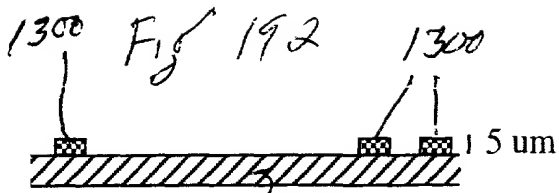


Fig. 11





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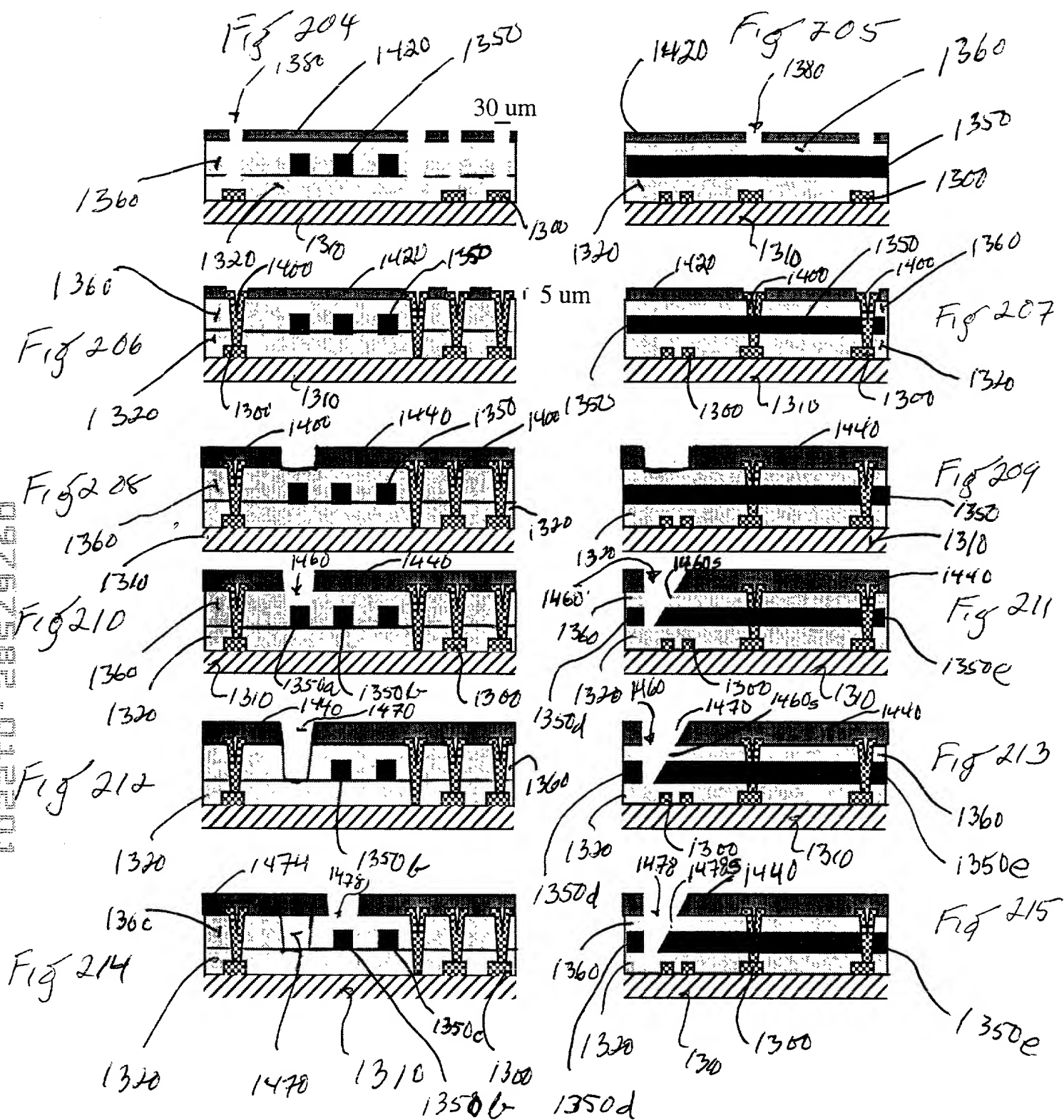


Fig 216

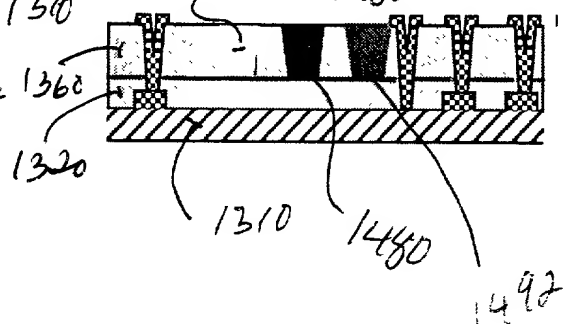
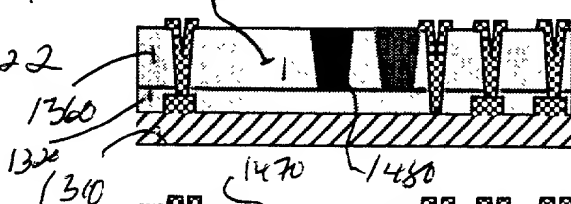
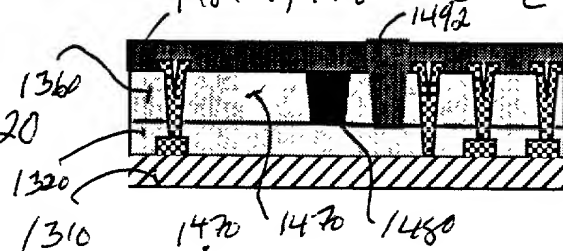
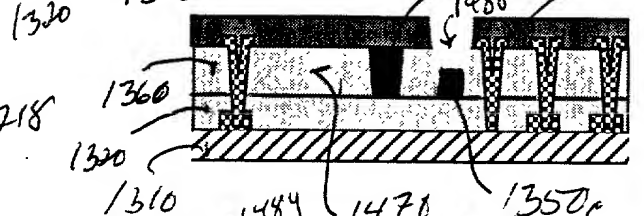
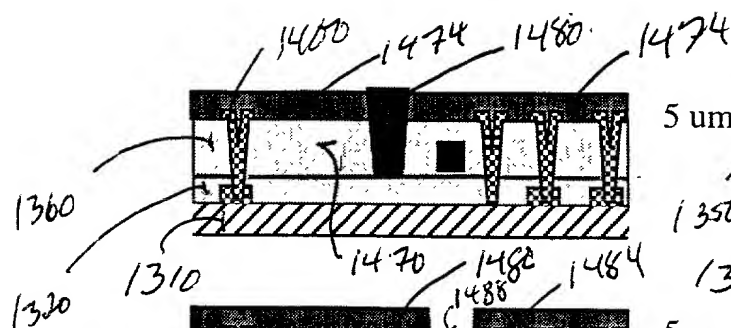


Fig 217

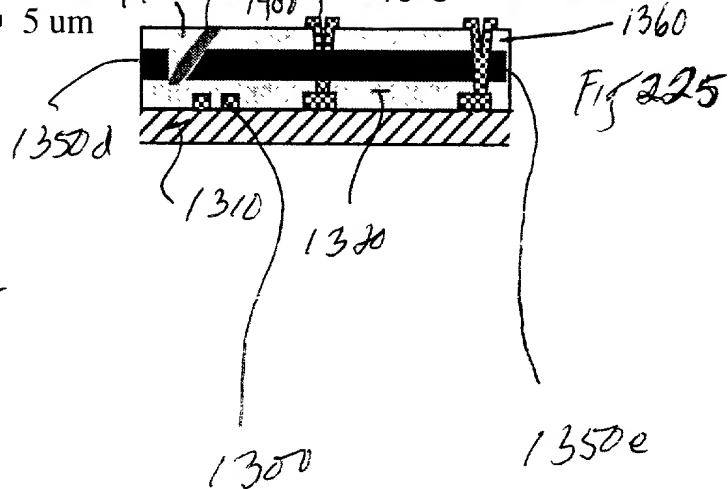
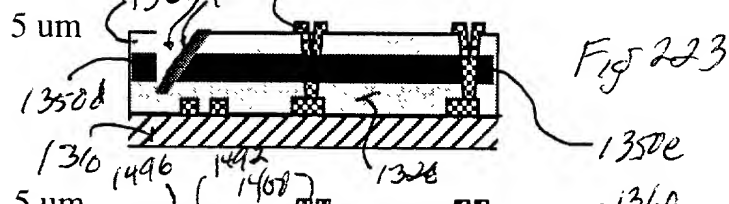
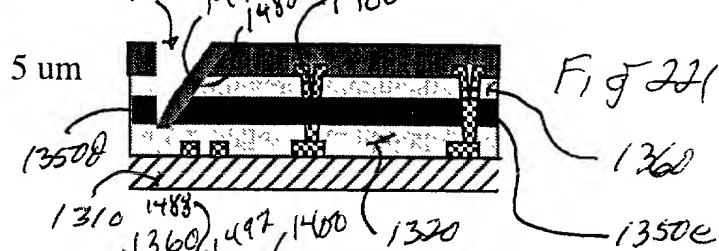
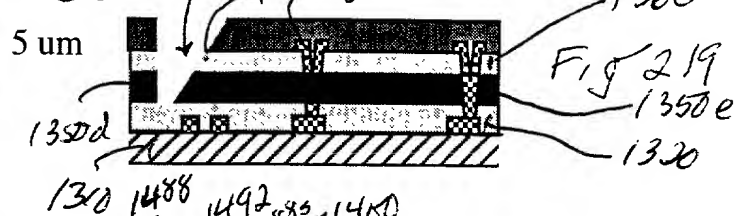
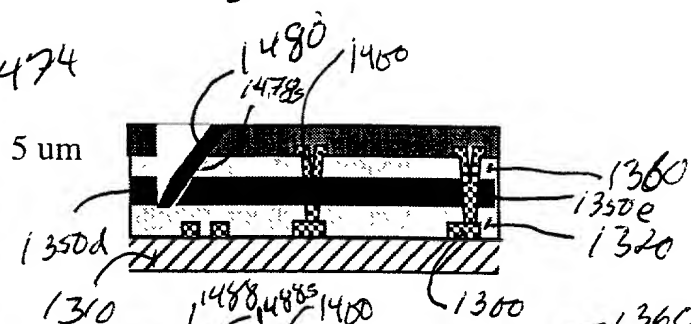


Fig 218

Fig 220

Fig 222

Fig 224

Fig 219

F, 5221

F19223

Fig 225

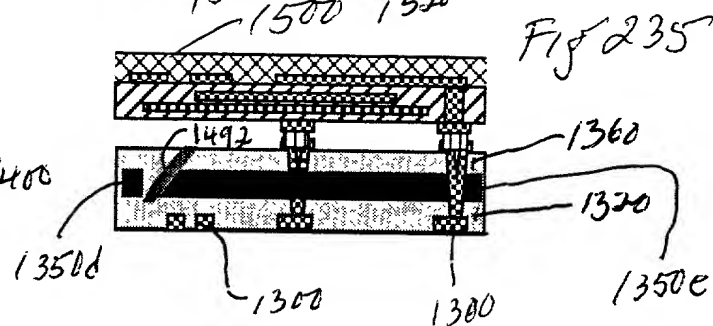
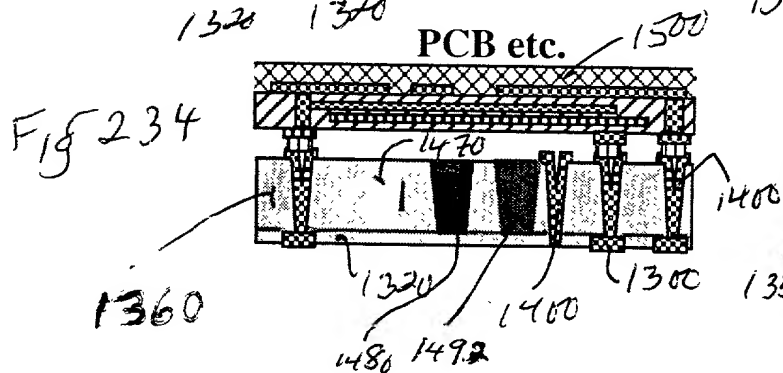
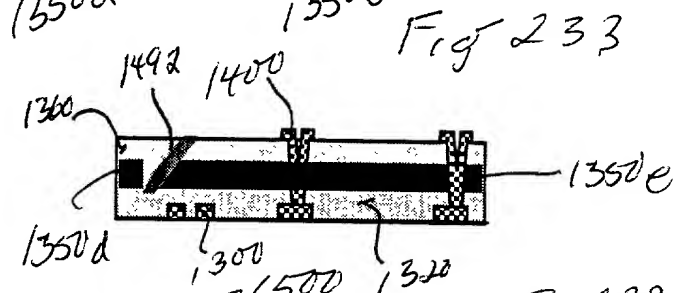
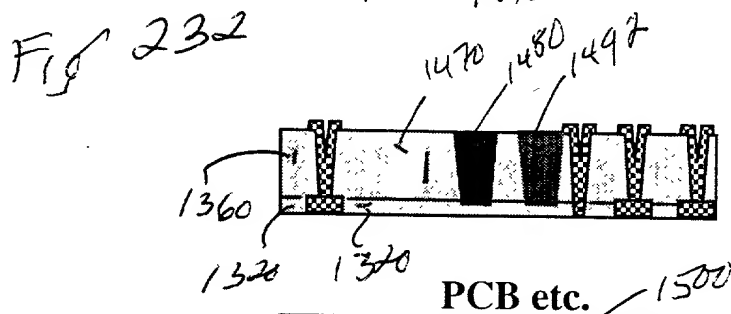
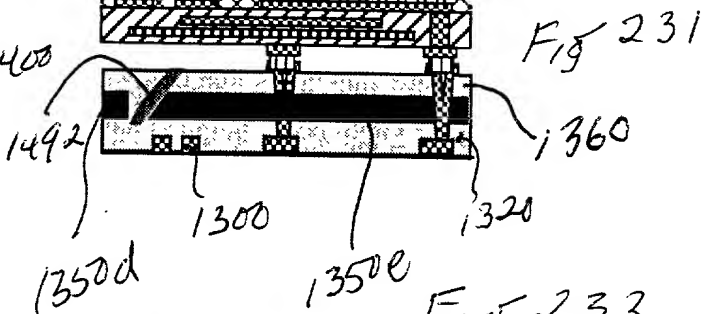
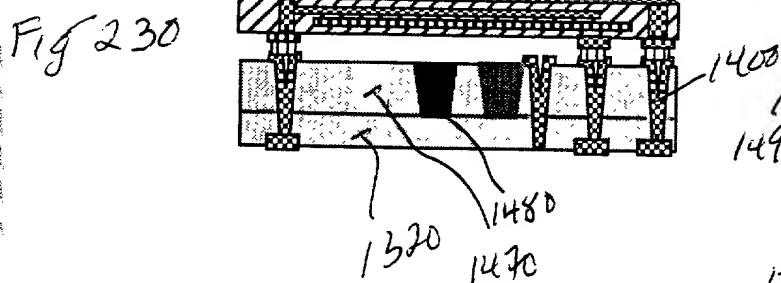
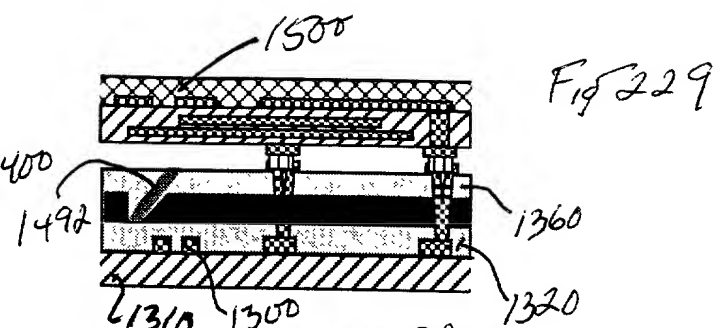
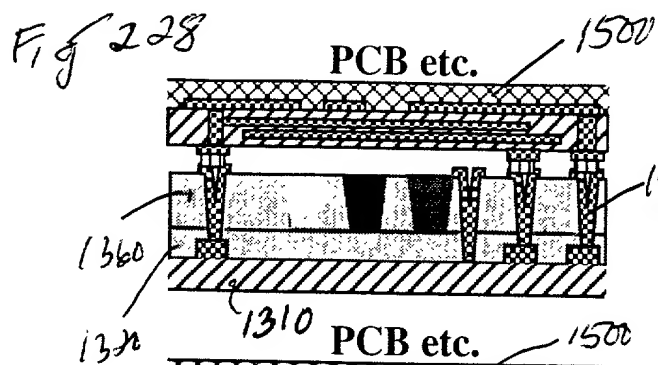
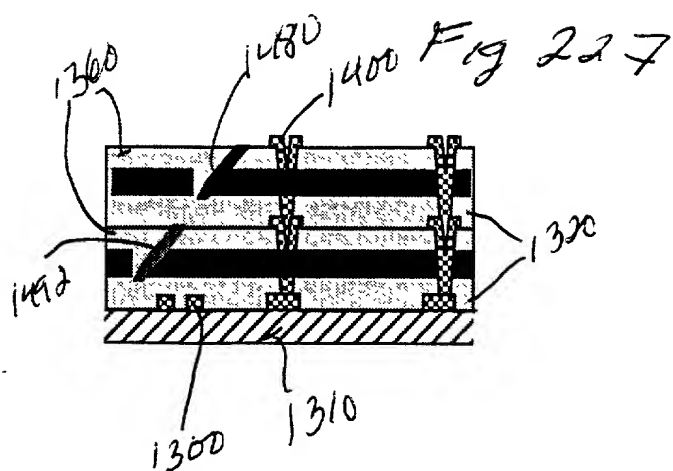
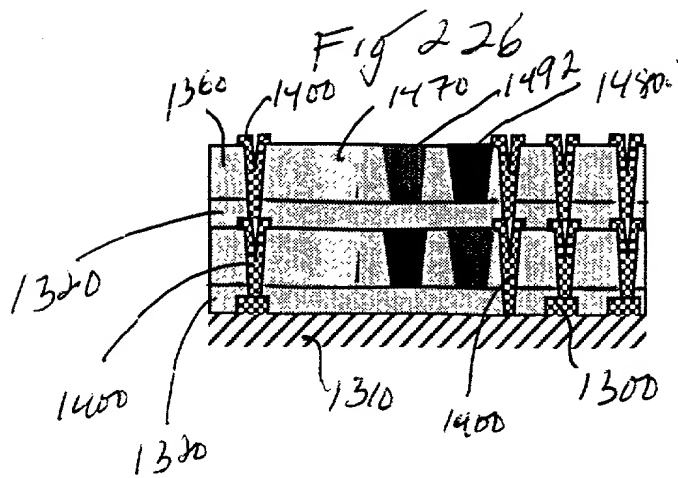


Fig 236

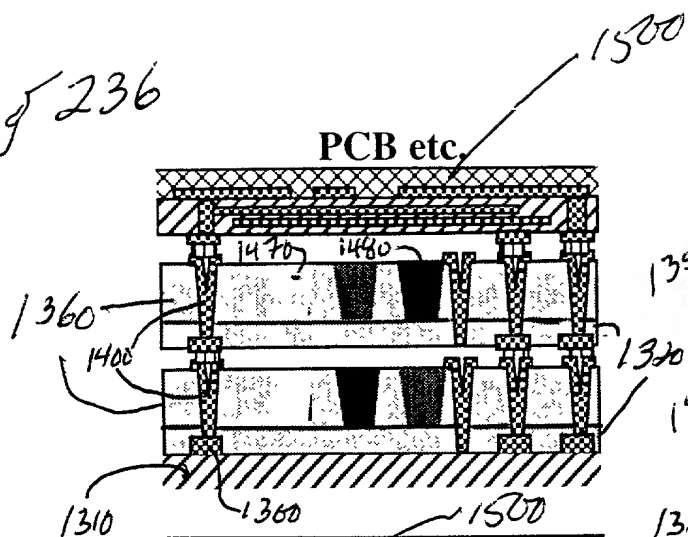


Fig 237

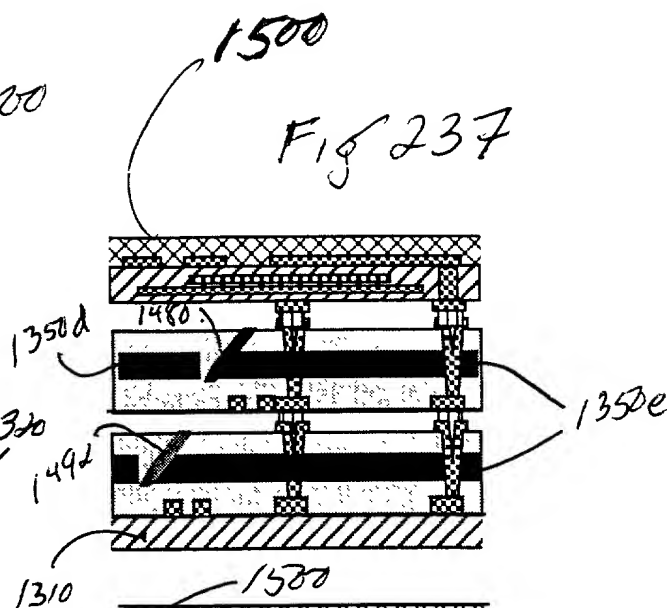


Fig 238

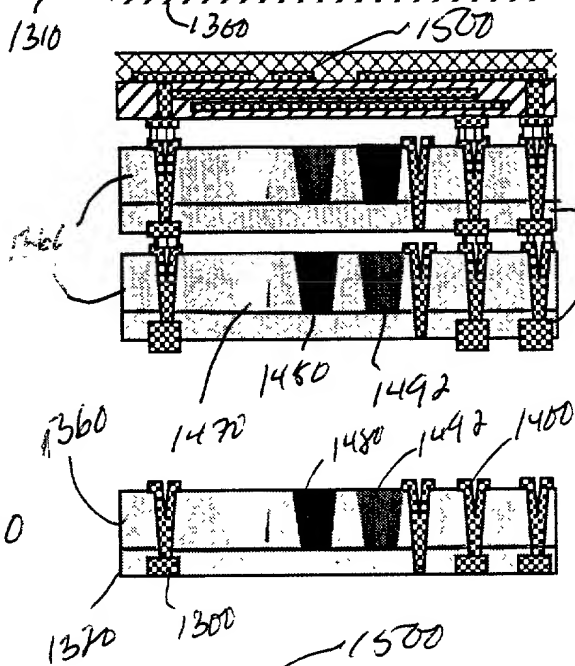


Fig 239

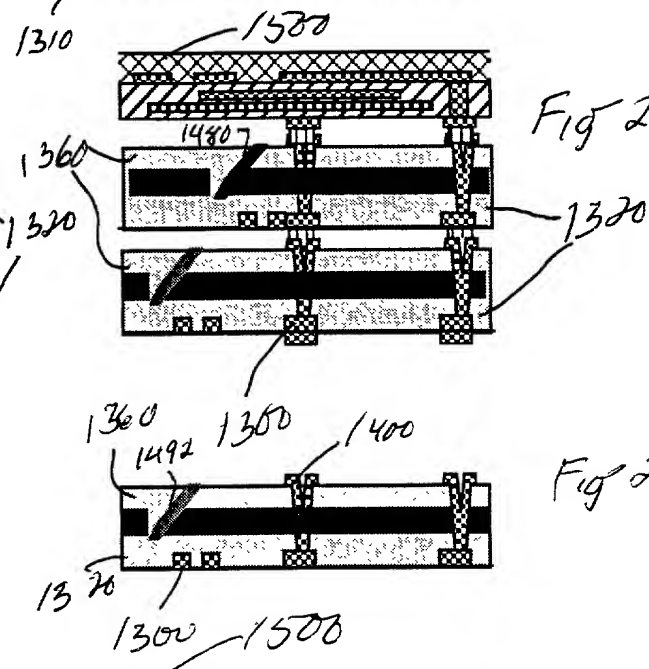


Fig 240

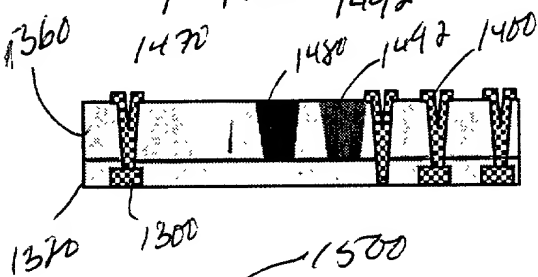


Fig 241

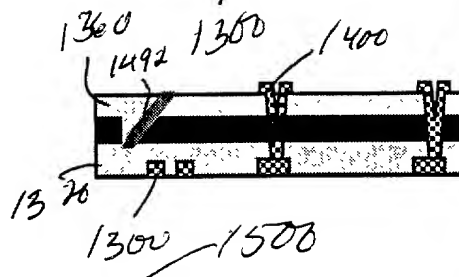


Fig 242

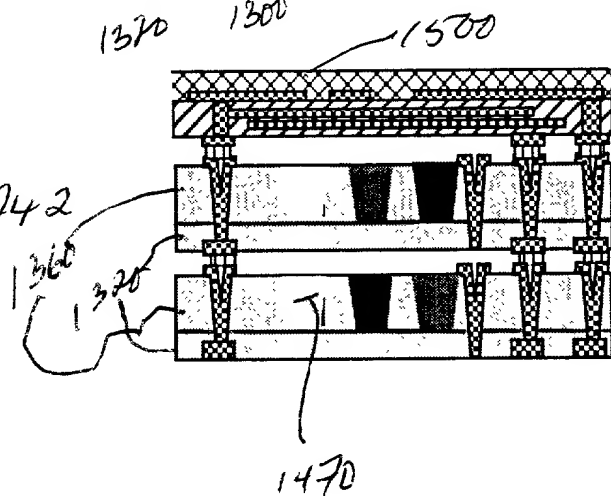


Fig 243

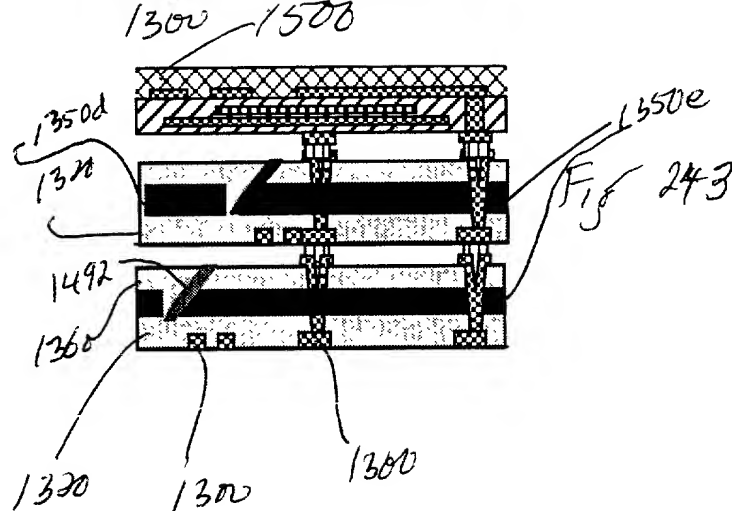


Fig 244



Fig 245

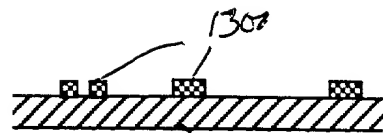


Fig 246

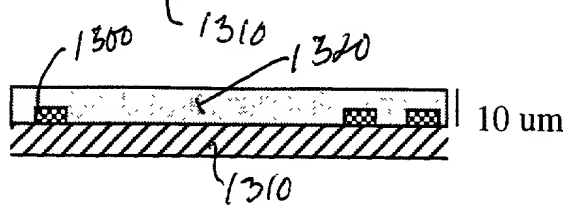


Fig 247

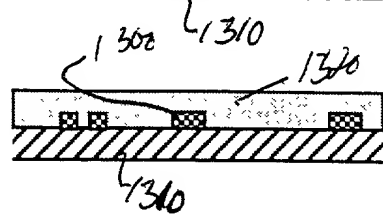


Fig 248

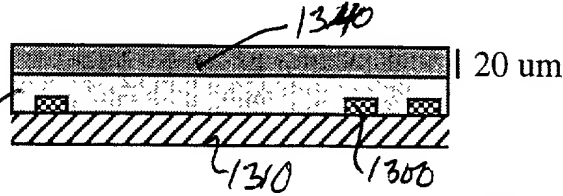
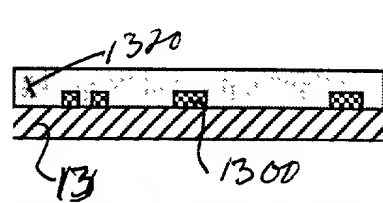


Fig 249



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Fig 250

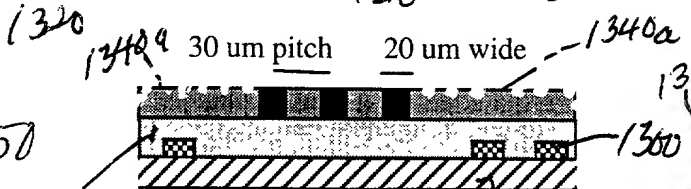


Fig 251

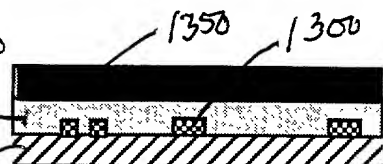


Fig 252

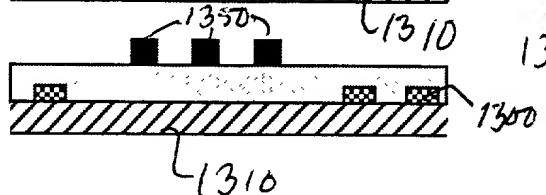


Fig 253

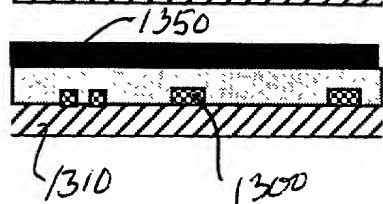


Fig 254

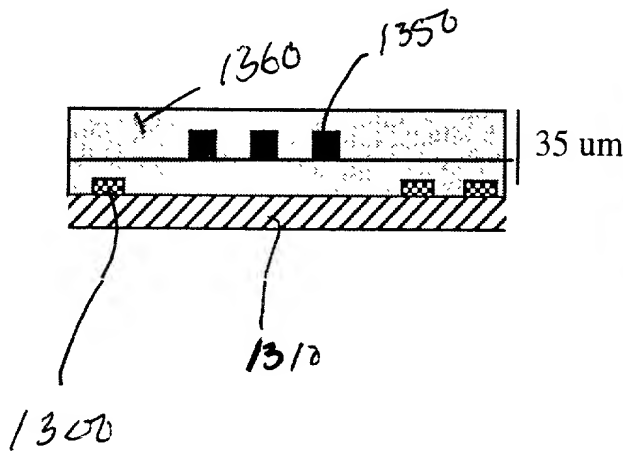
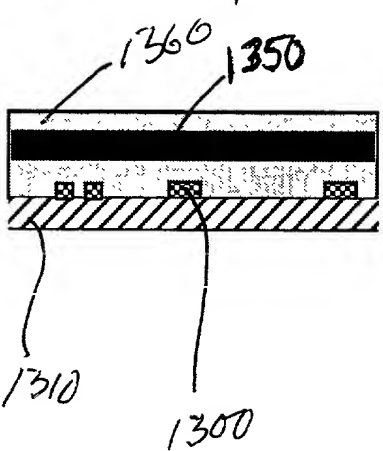


Fig 255



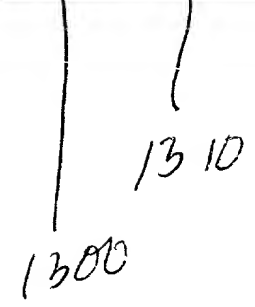
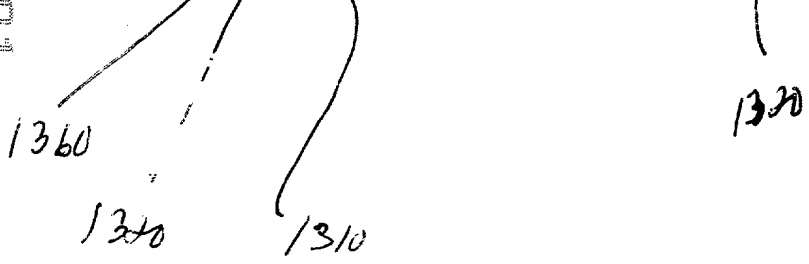
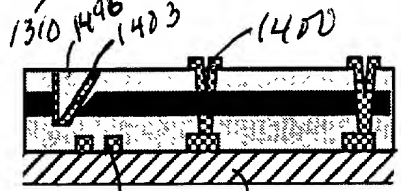
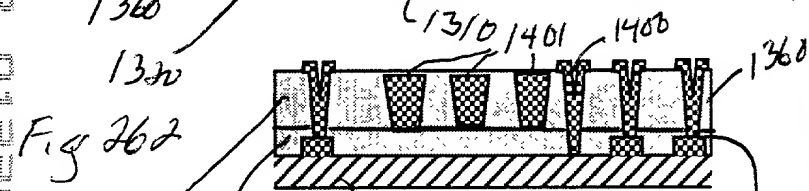
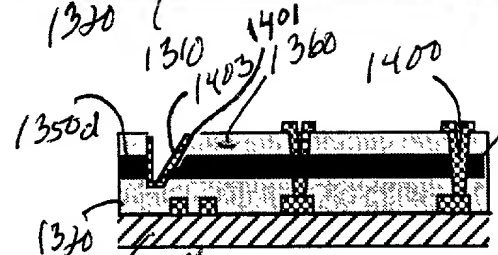
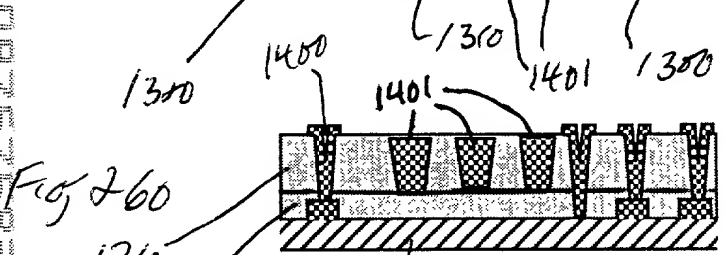
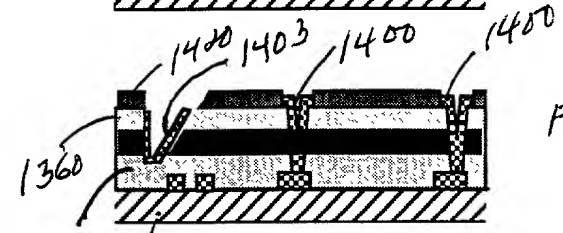
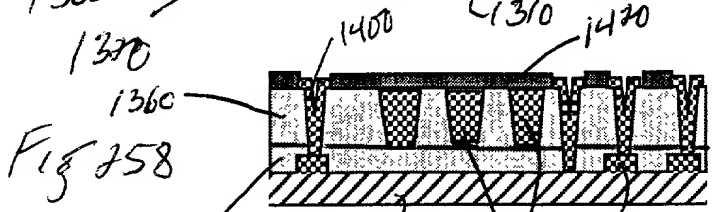
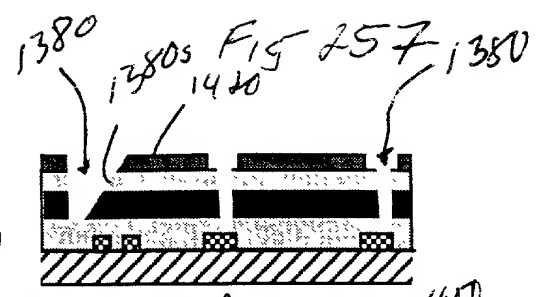
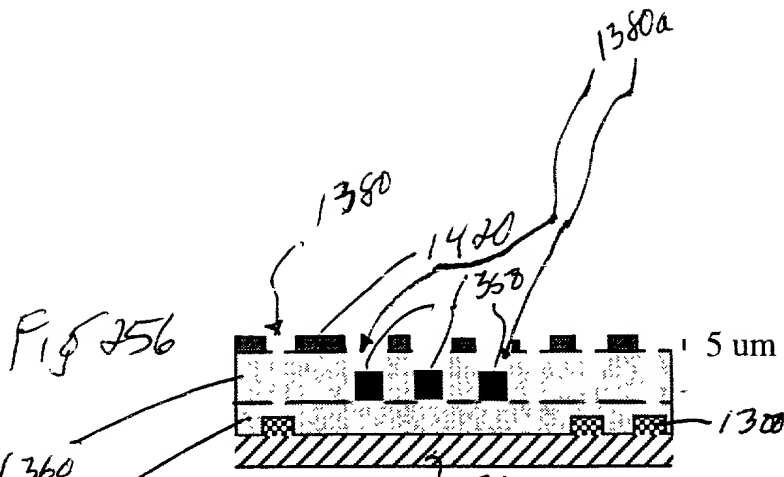


Fig 264

1360

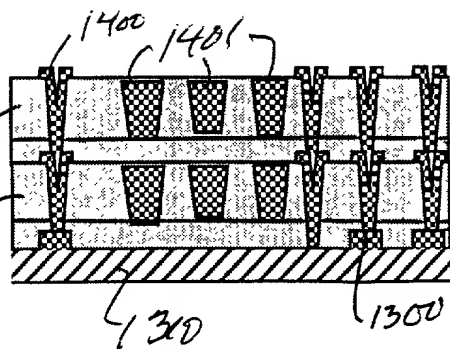


Fig 265

1320

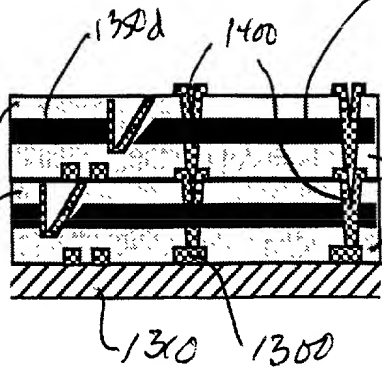


Fig 266

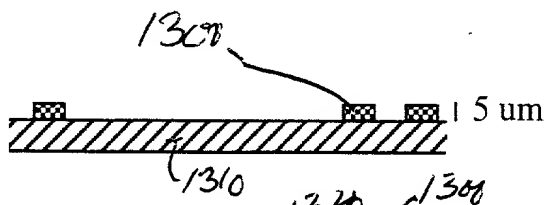


Fig 267

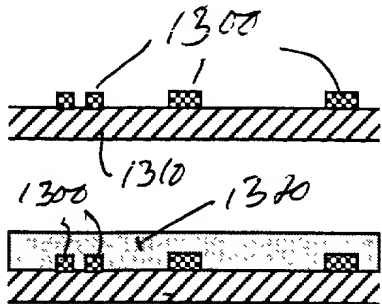


Fig 268



Fig 269

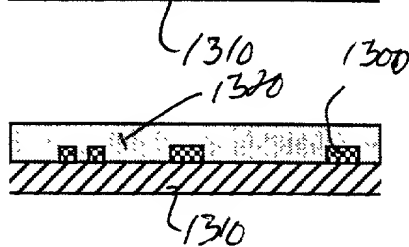


Fig 270

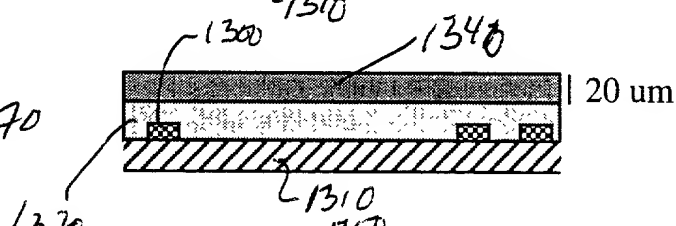


Fig 271

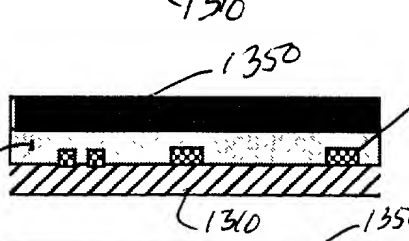


Fig 272

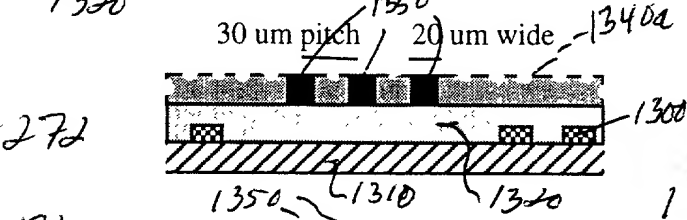


Fig 273

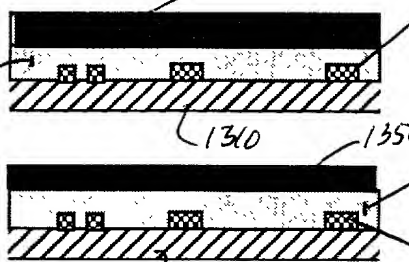


Fig 274

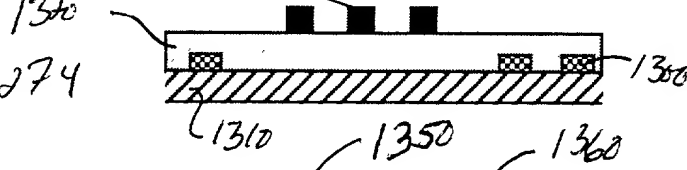


Fig 275

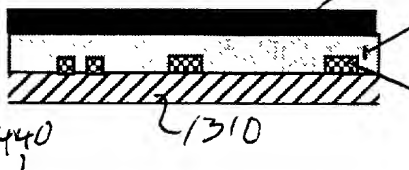


Fig 276

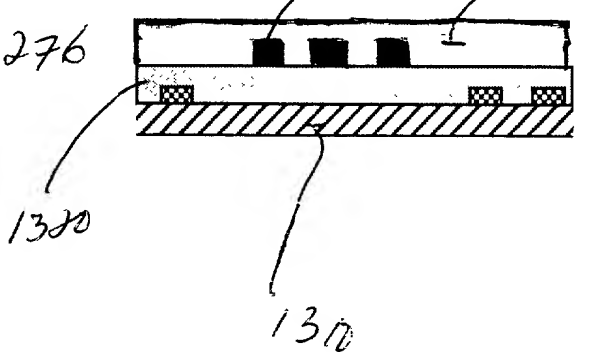
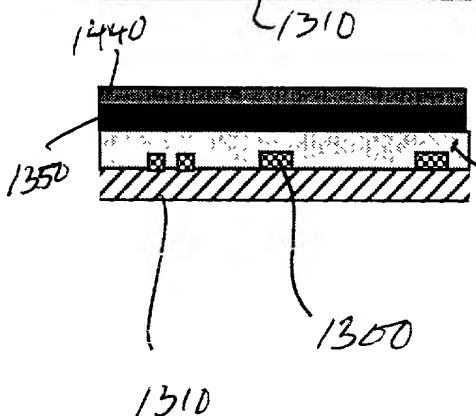
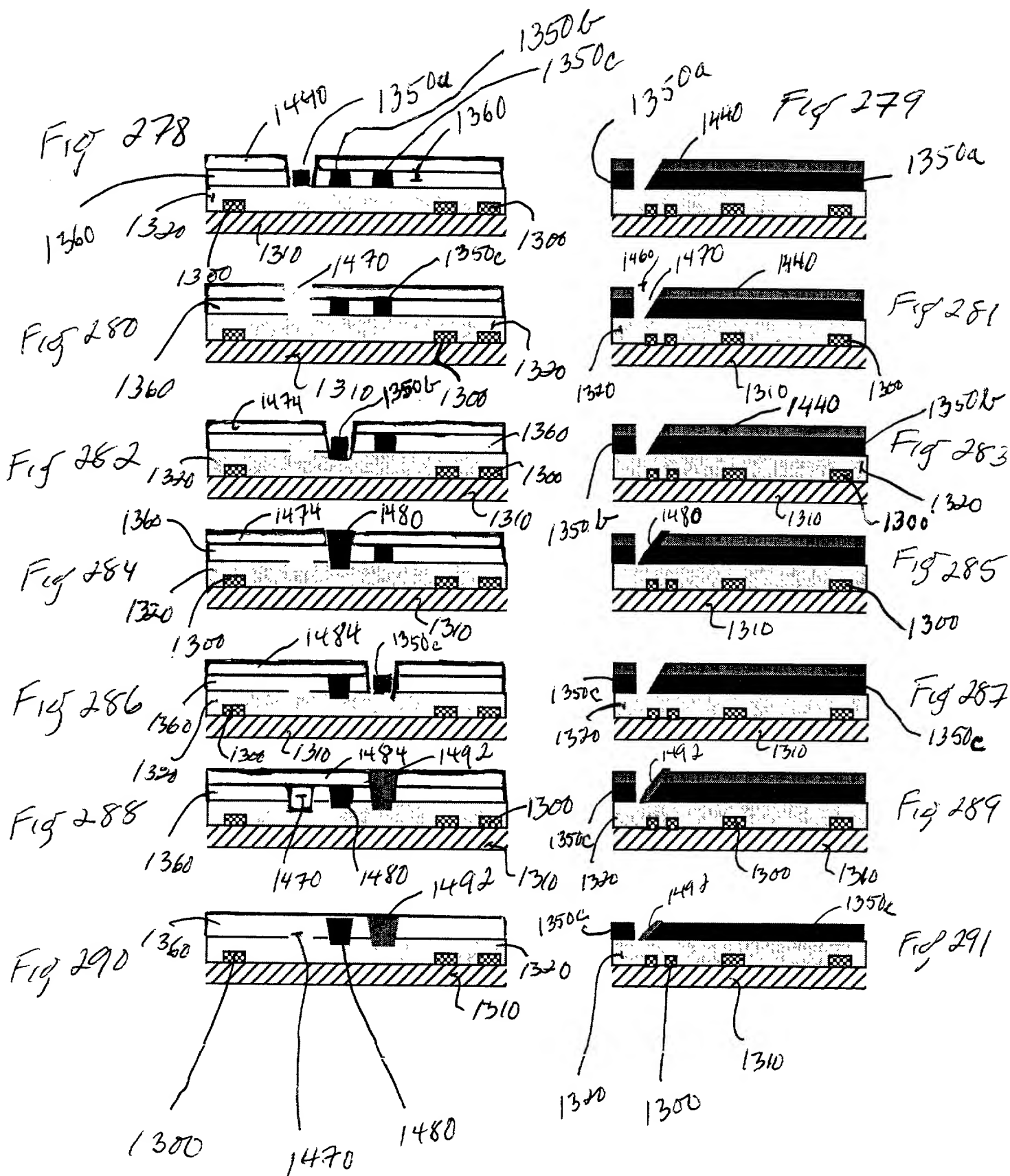


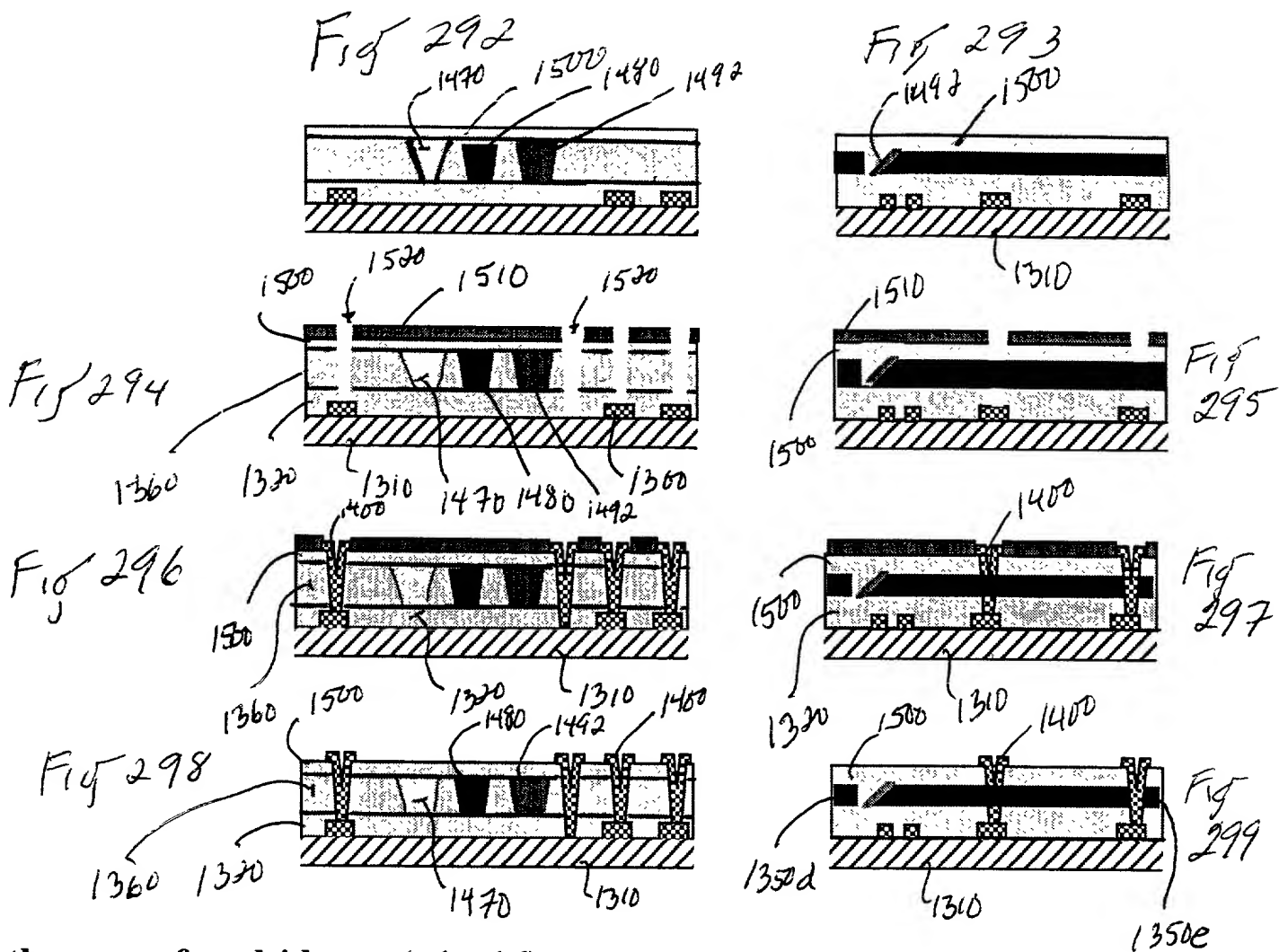
Fig 277





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In the case of multi layer (a1-a16) process is repeated on the (a16).

-it is also possible to repeat (a3-a16) or (a1, a3-a16)

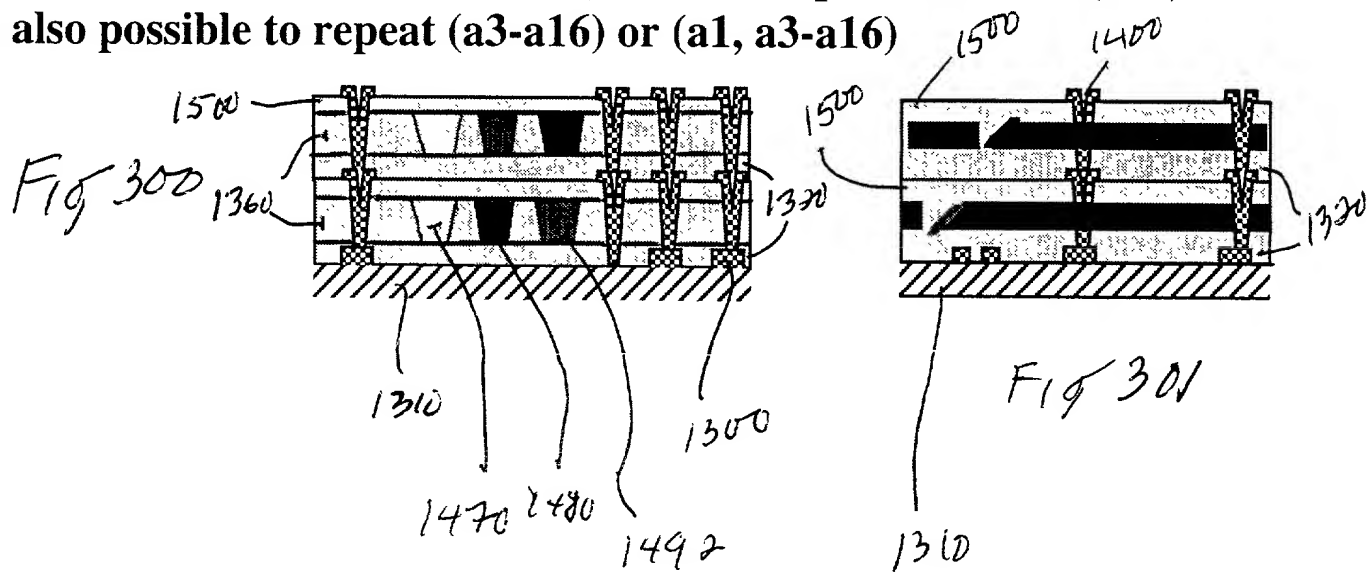


Fig 302

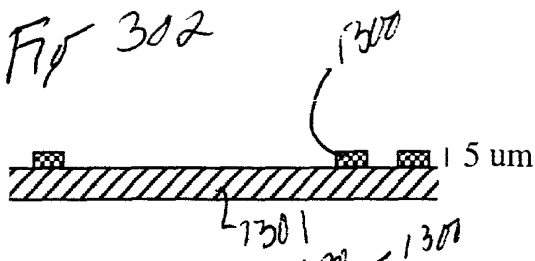


Fig 303

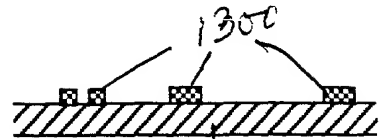


Fig 304

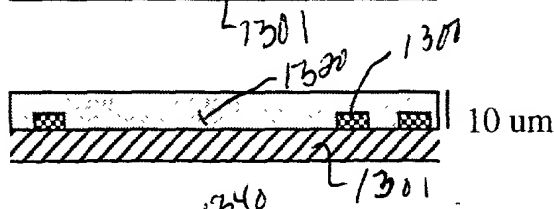


Fig 306

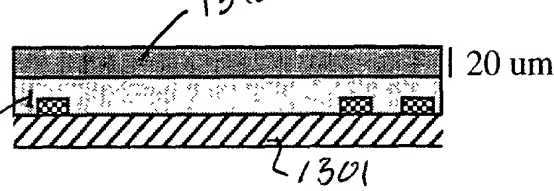


Fig 308

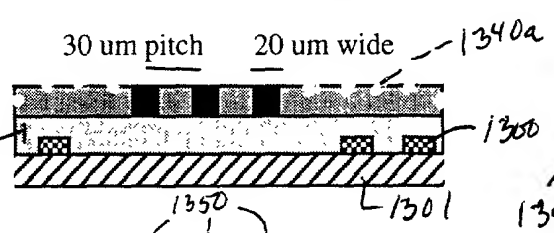


Fig 310

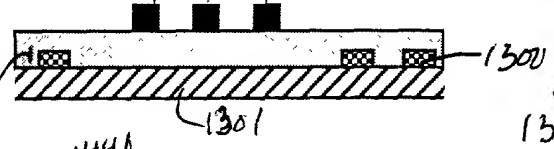


Fig 312

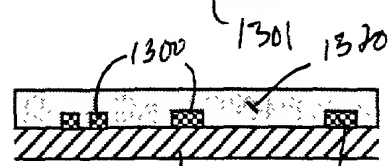


Fig 305

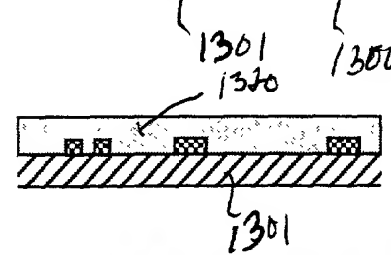


Fig 307

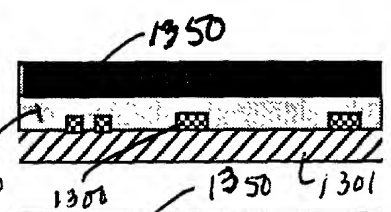


Fig 309

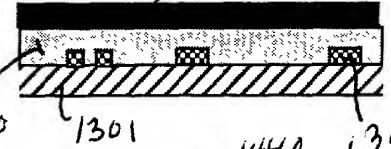
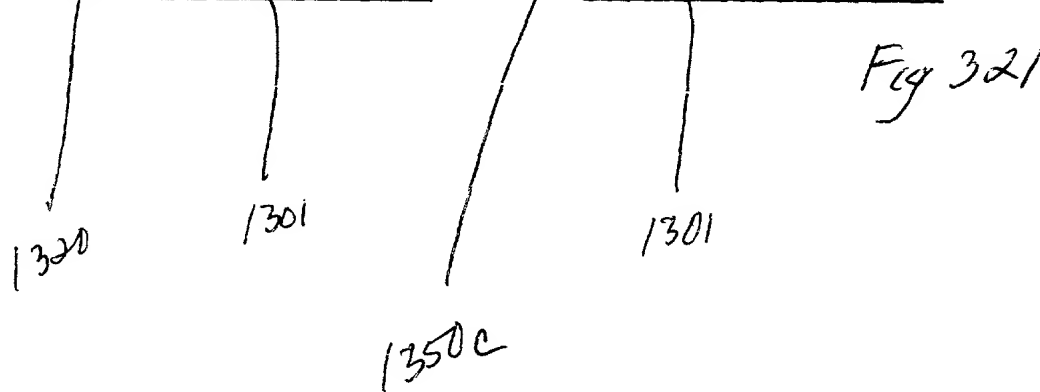
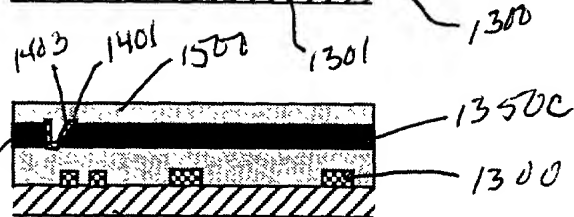
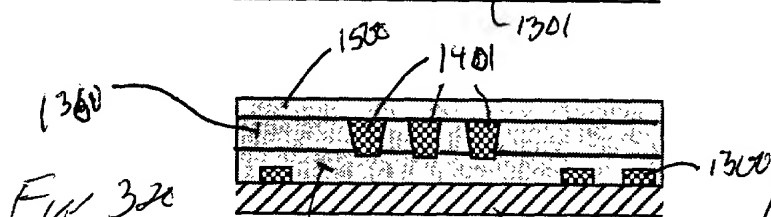
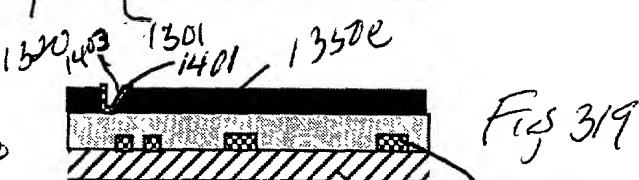
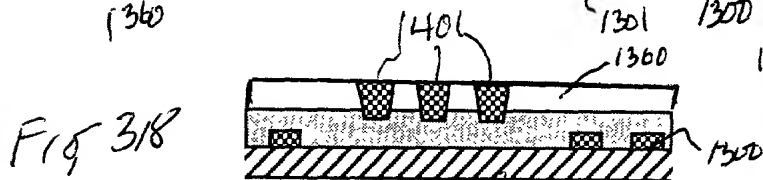
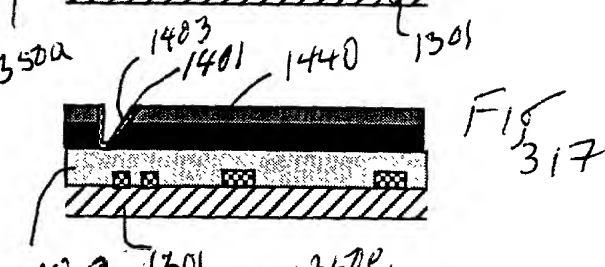
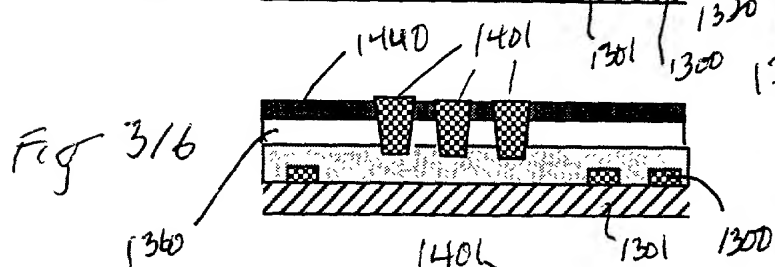
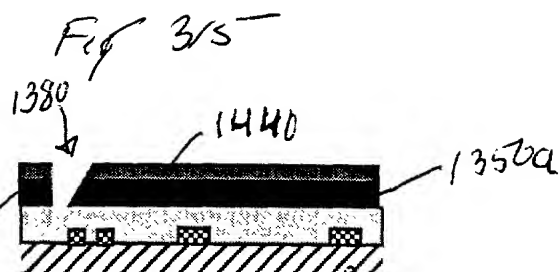
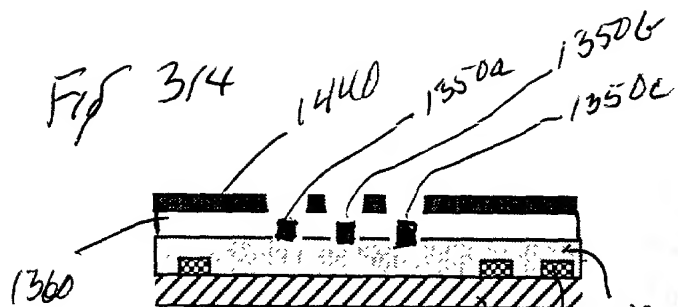


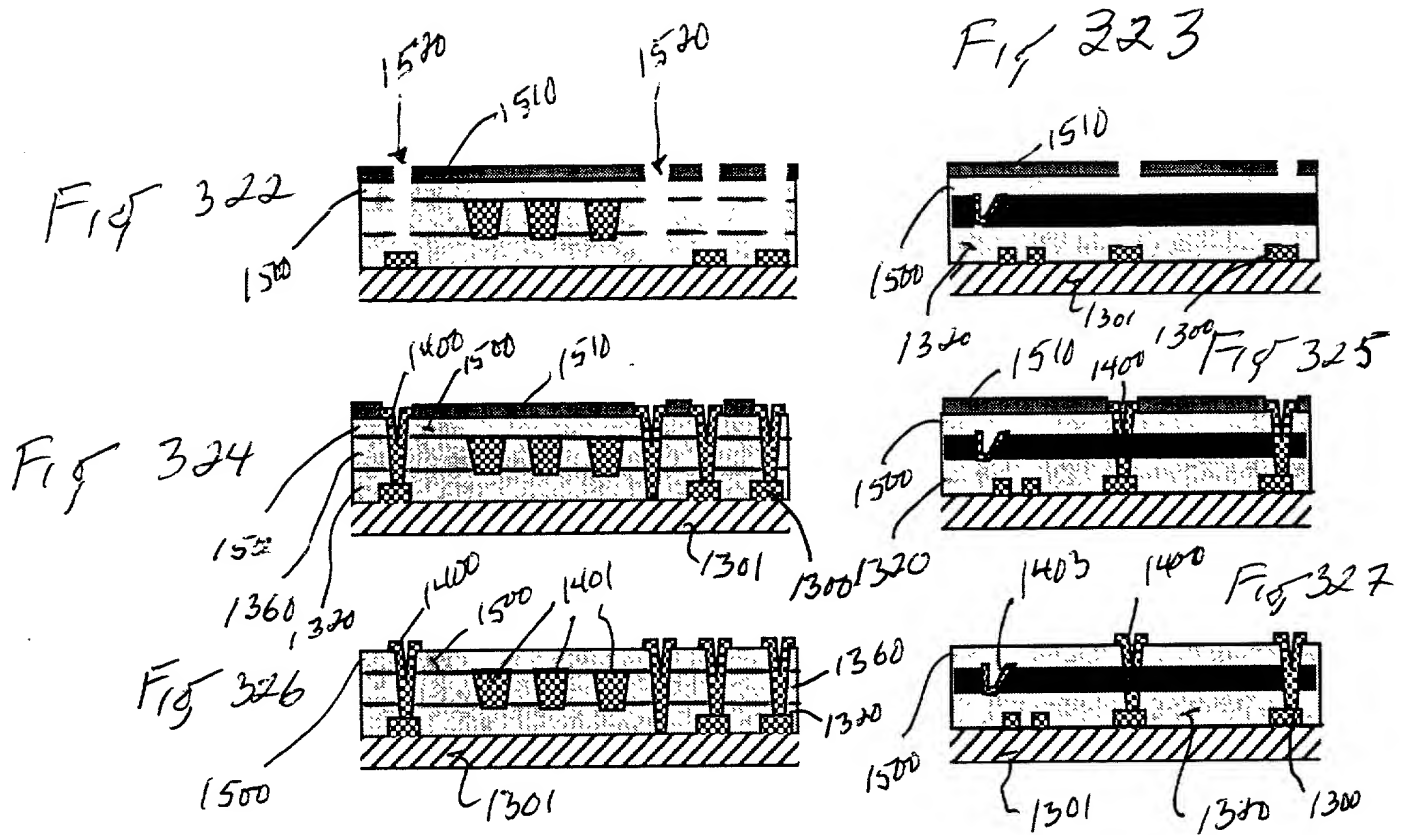
Fig 311



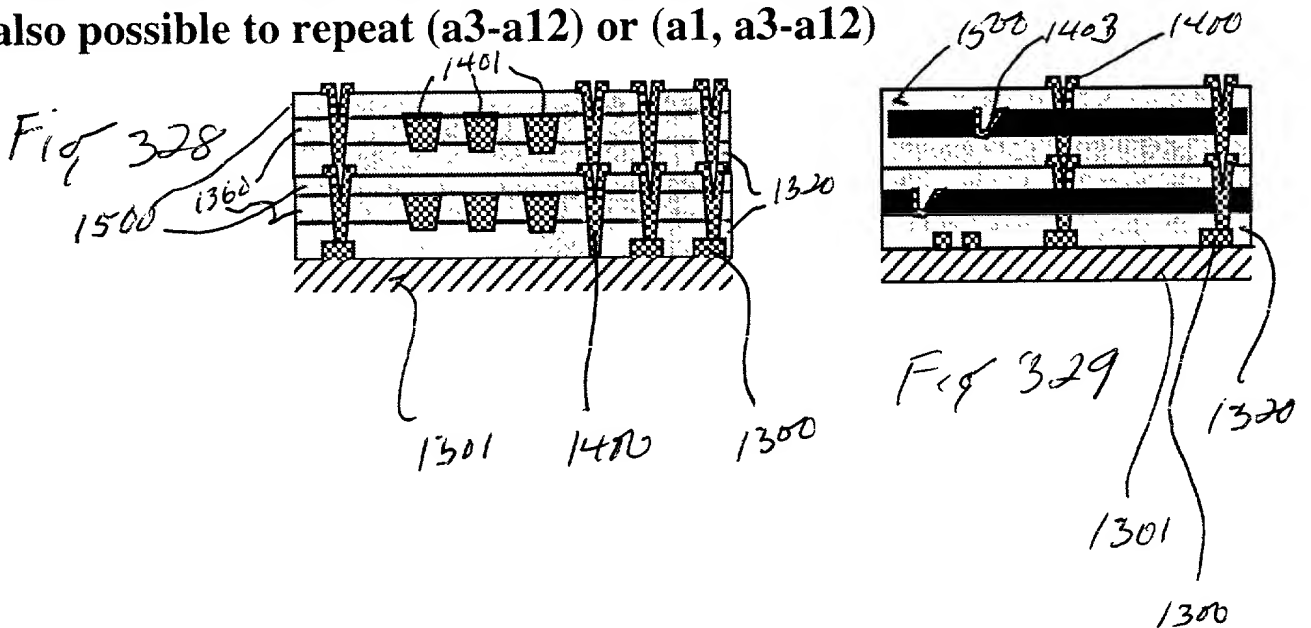
Fig 313

09767588.01301





In the case of multi layer (a1-a12) process is repeated on the (a12).  
 -it is also possible to repeat (a3-a12) or (a1, a3-a12)



# Invented Corner Turning Structure (A)

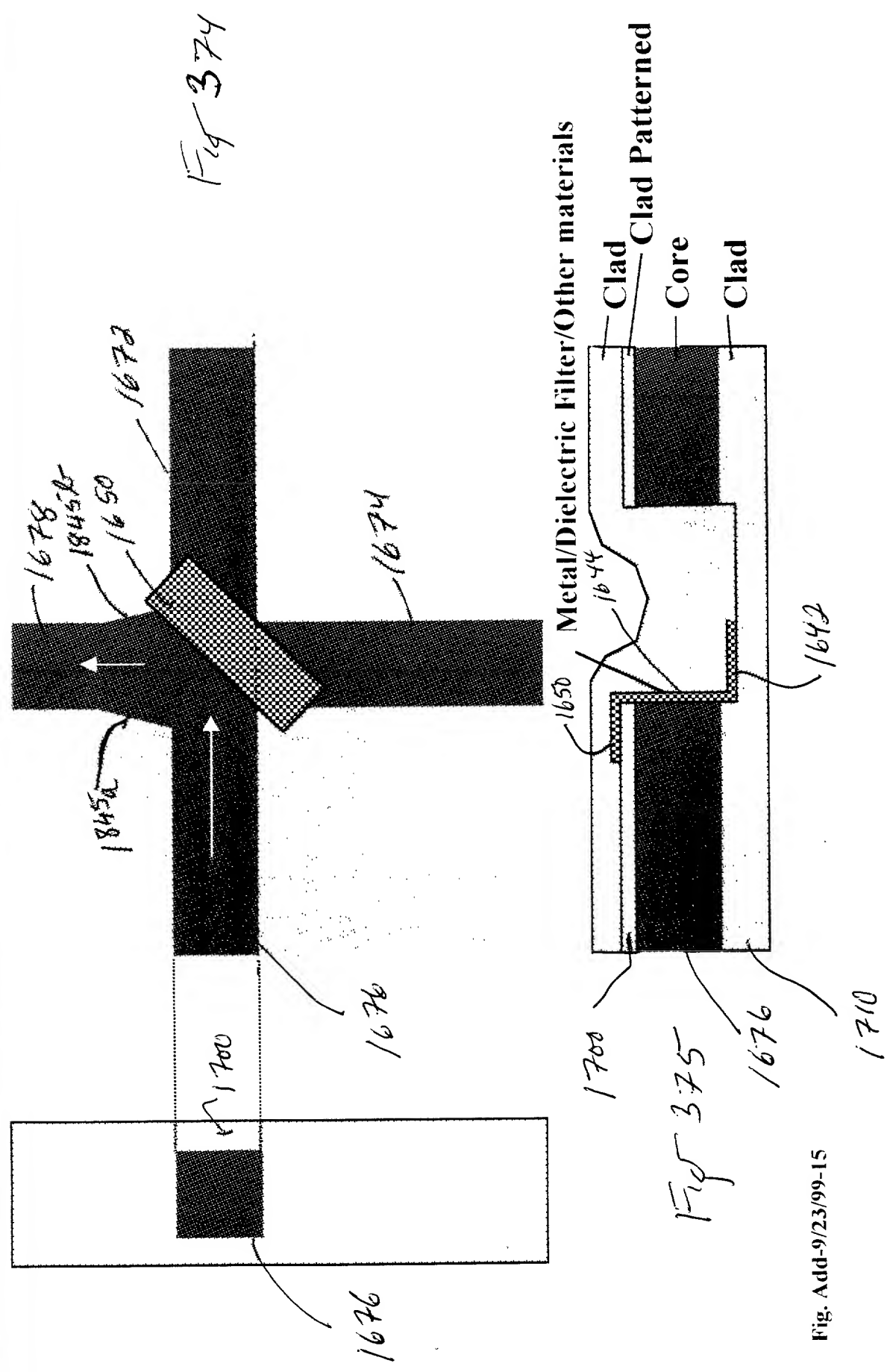
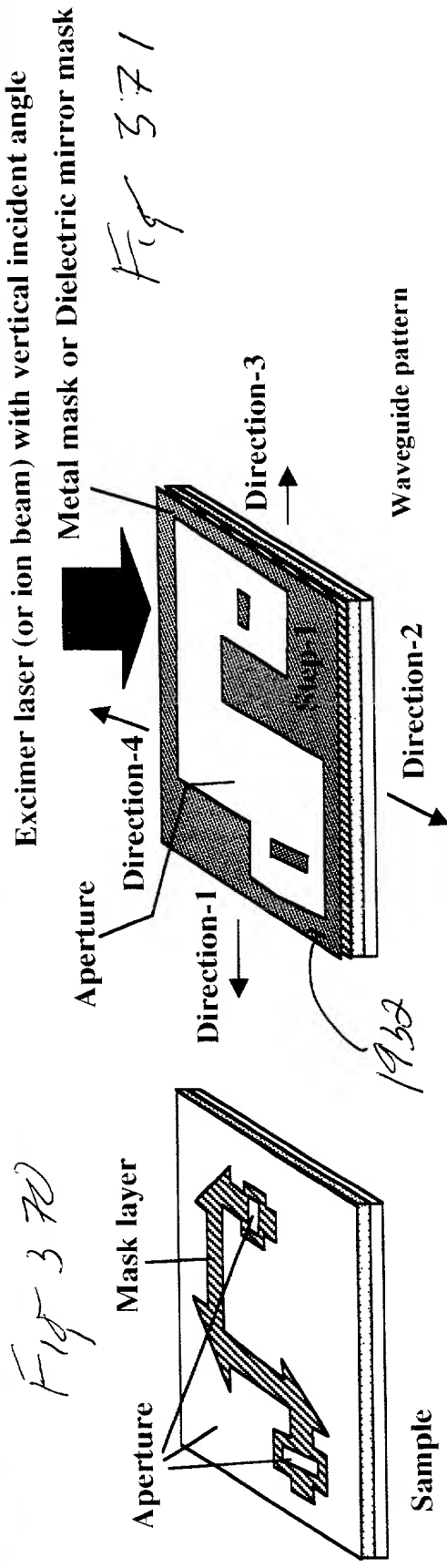
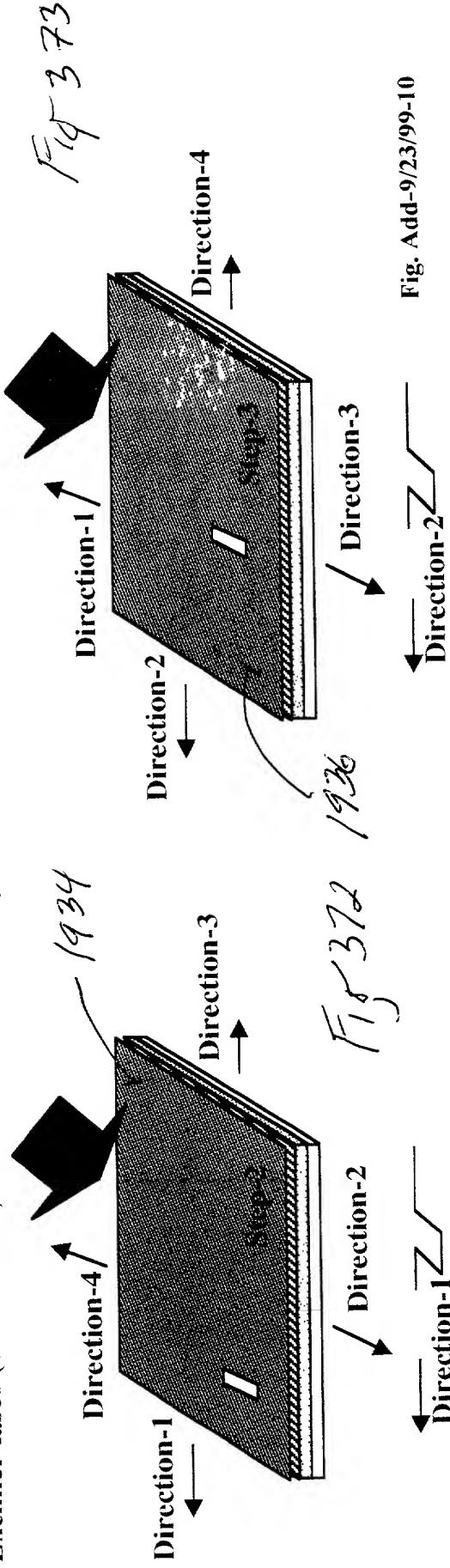


Fig. Add-9/23/99-15

# MNA, MNE Example for Add2 example



Excimer laser (or ion beam) with tilted incident angle



# Another Process Flow for Structure (II)

Fig 350

Buffer/Clad/Core/Clad Waveguide Formation

Mask formation For Waveguide/Coupler

MNA or MNE Aperture

Fig 350

Fig 351

Fig 352

Fig 353

Fig 354

Fig 355

Fig 356

Fig 357

Fig 358

Fig 359

Fig 360

Fig 361

Fig 362

Fig 363

Fig 364

Fig 365

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Fig 380

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Fig 382

Fig 383

Fig 384

Fig 385

Coupler Formation I

MNA or MNE

Aperture

Fig 357

Fig 358

Fig 359

Fig 360

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Fig 380

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Fig 382

Fig 383

Fig 384

Fig 385

Coupler Formation II

MNA or MNE

Aperture

Fig 363

Fig 364

Fig 365

Fig 366

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Fig 368

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Fig 371

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Fig 373

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Fig 383

Fig 384

Fig 385

Metallization

Fig 360

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Fig 362

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Fig 363

Fig 364

Fig 365

&lt;



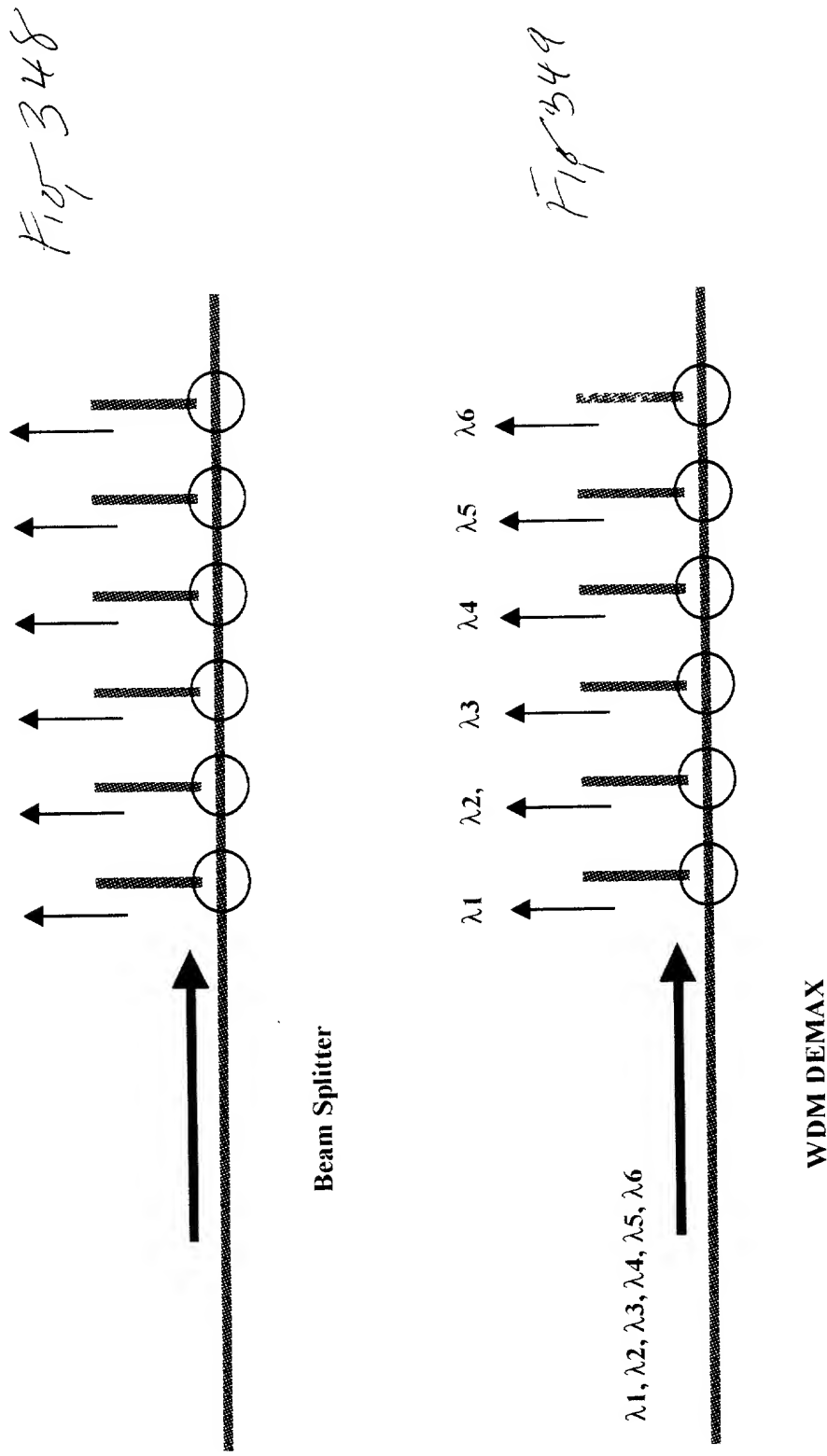


Fig. Add-9/23/99-8

# Invented Coupler Structure (II)

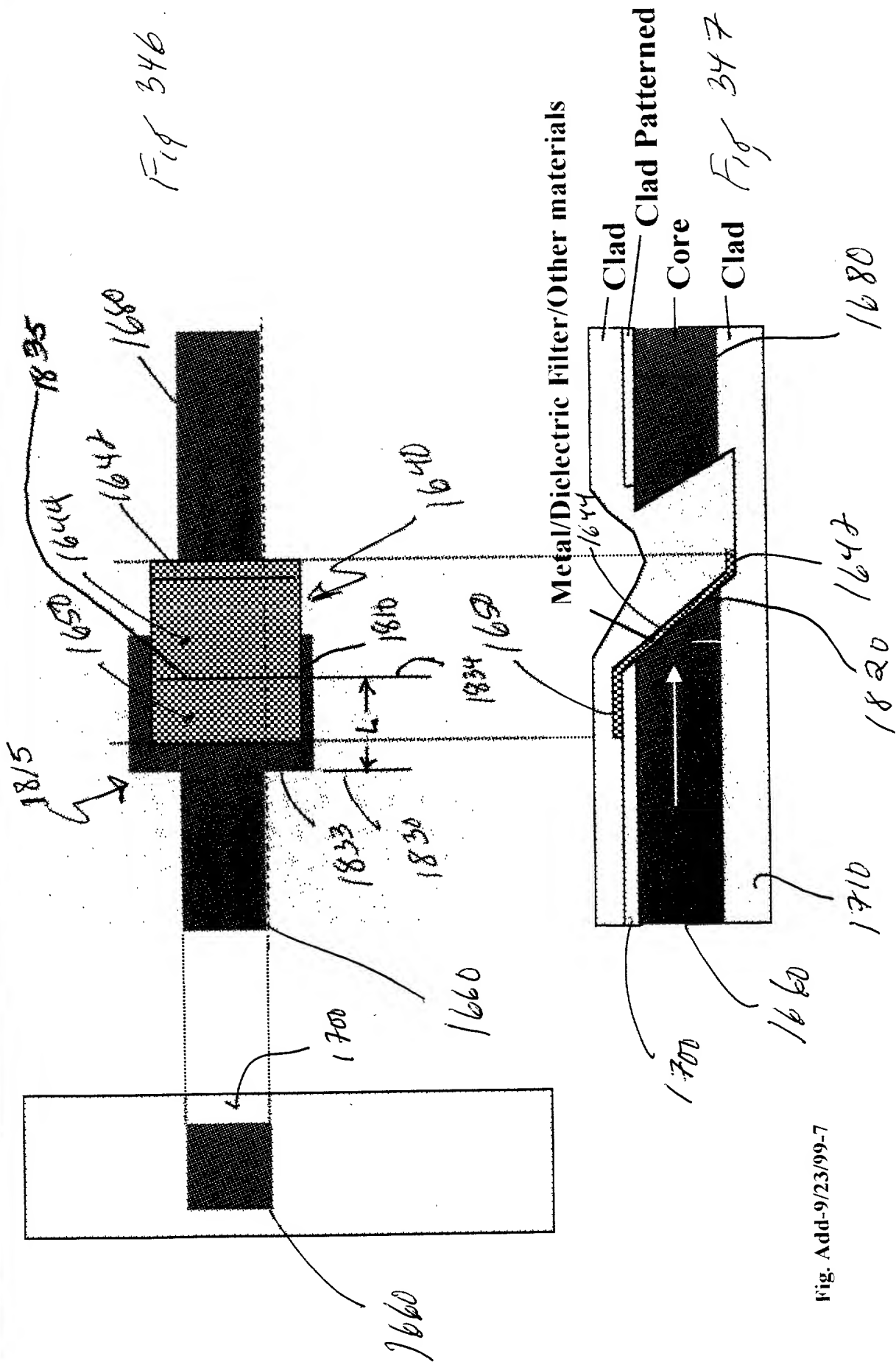


Fig. Add-9/23/99-7

# Invented Coupler Structure (I)

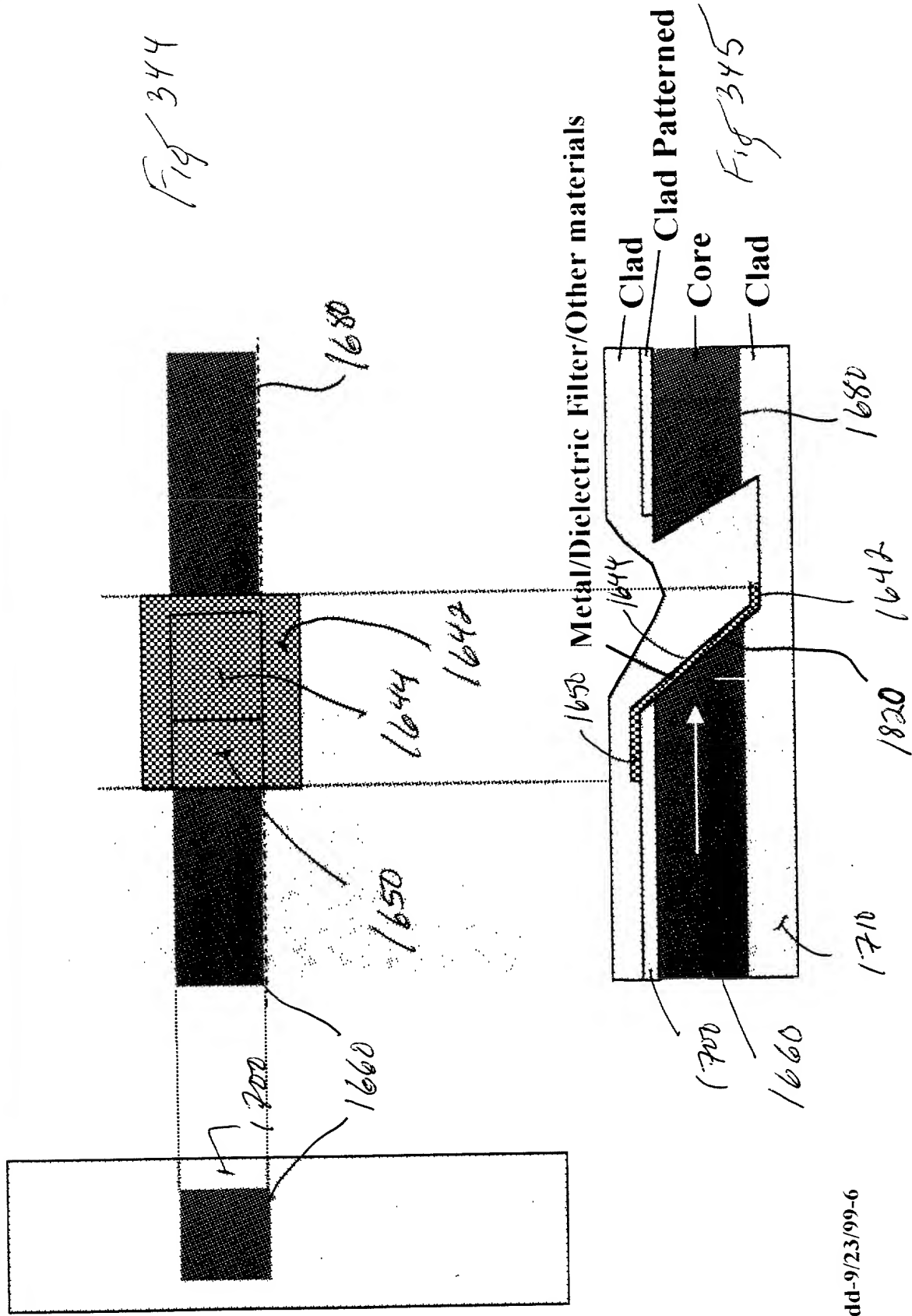
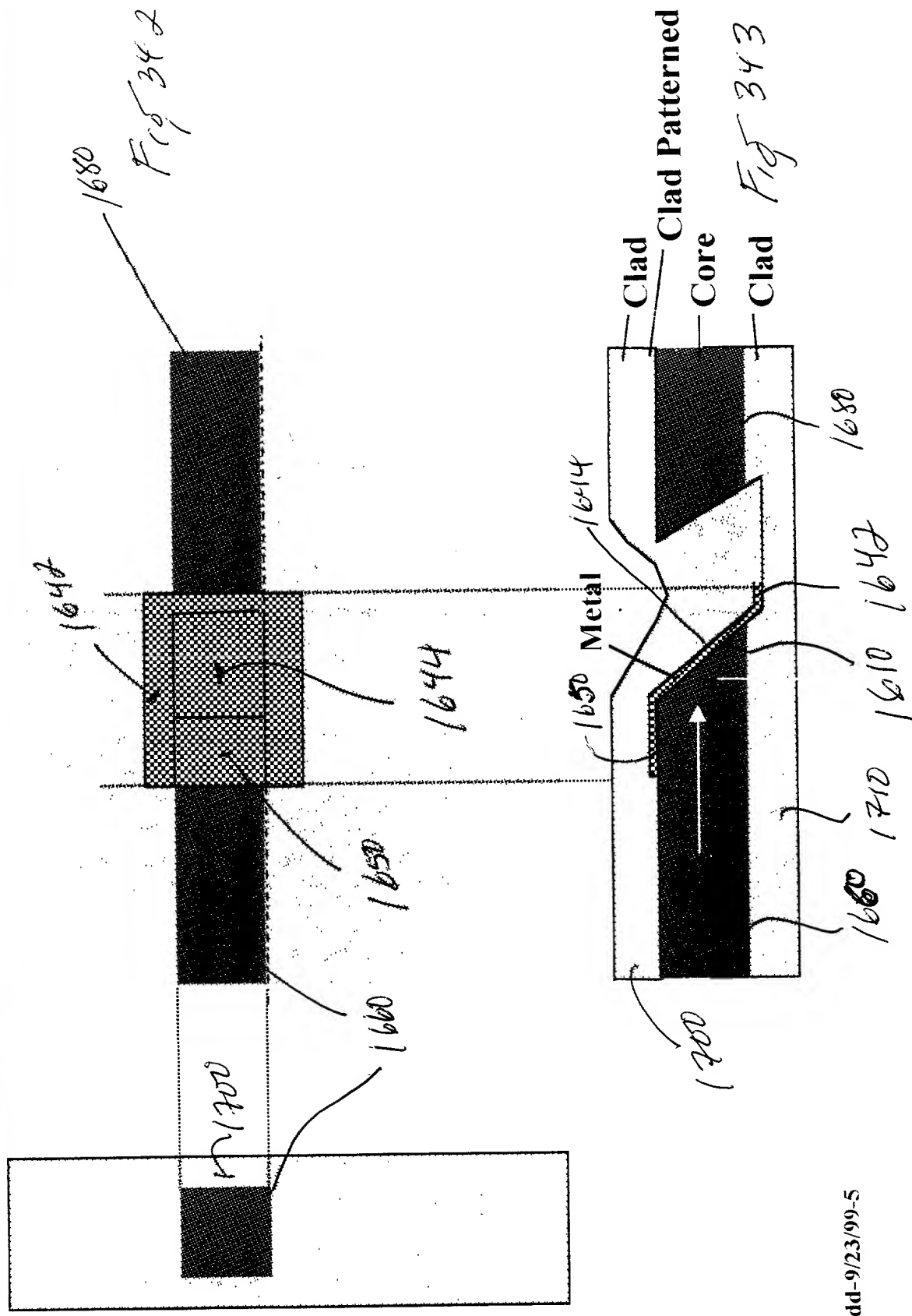


Fig. Add-9/23/99-6

## Conventional Coupler Structure (I)



**Fig. Add-9/23/99-5**

# Invented Corner Turning Structure (II)

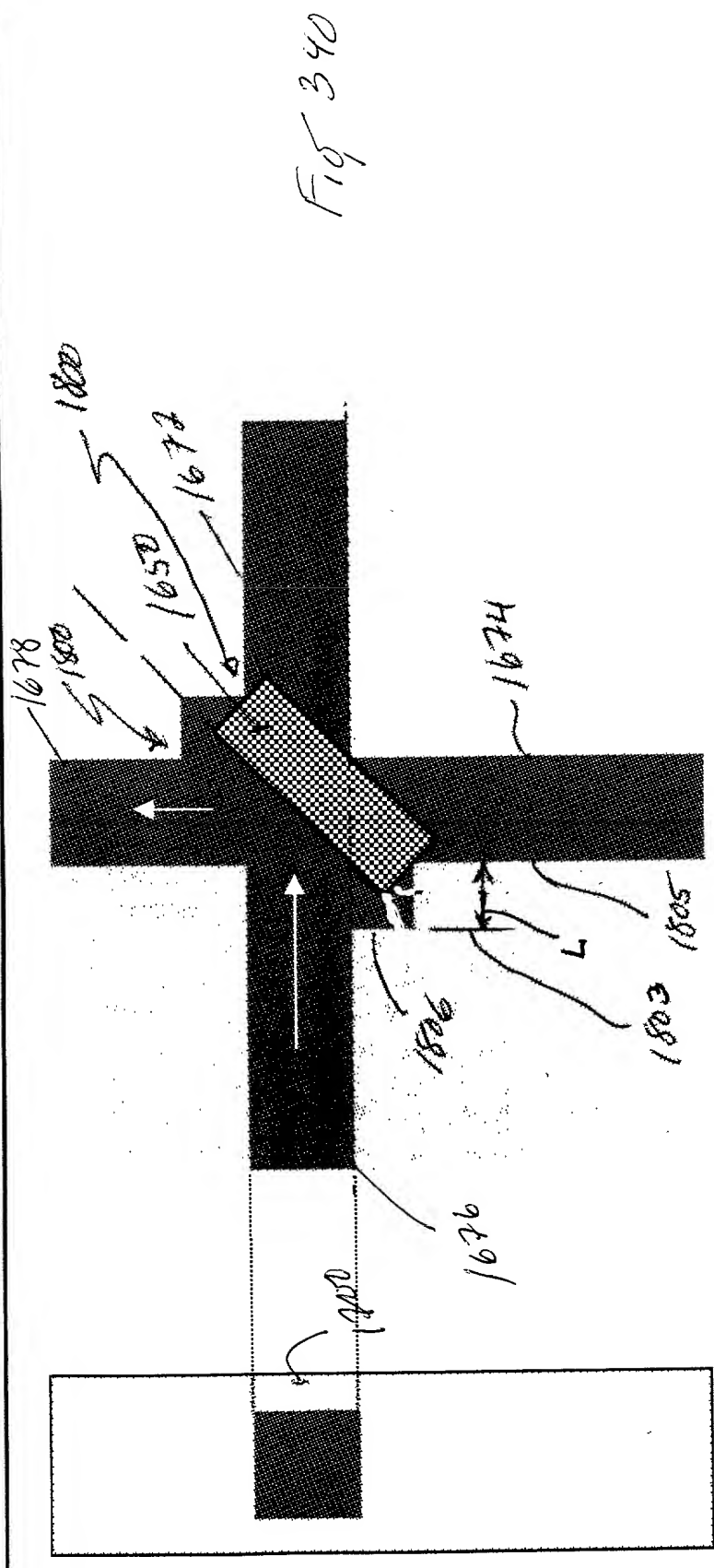


Fig. 340

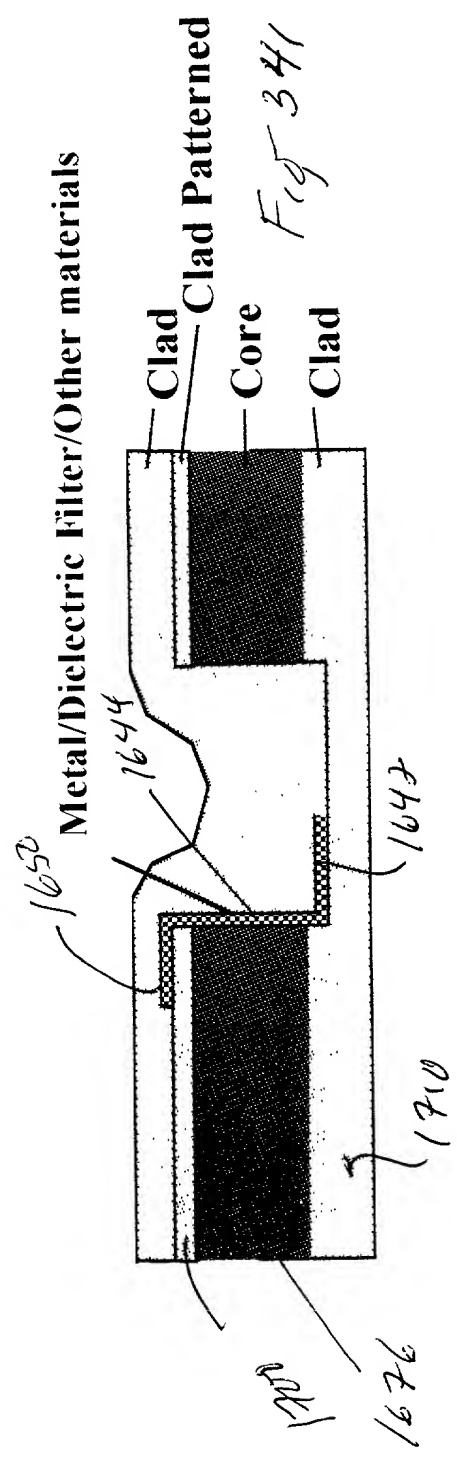


Fig. 341

Fig. Add-9/23/99-4

# Invented Corner Turning Structure (I)

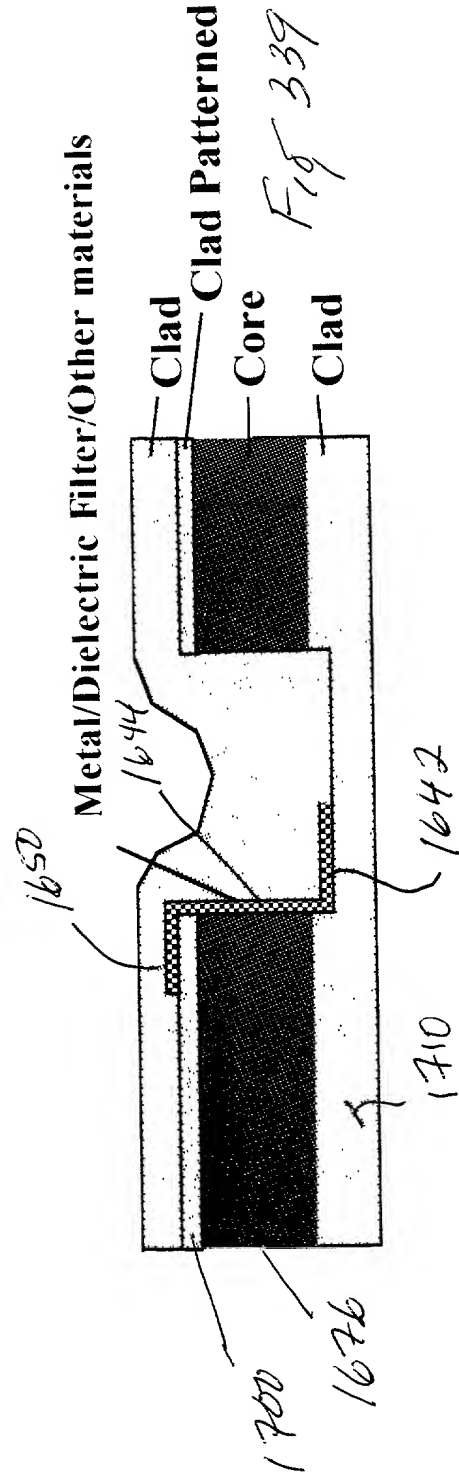
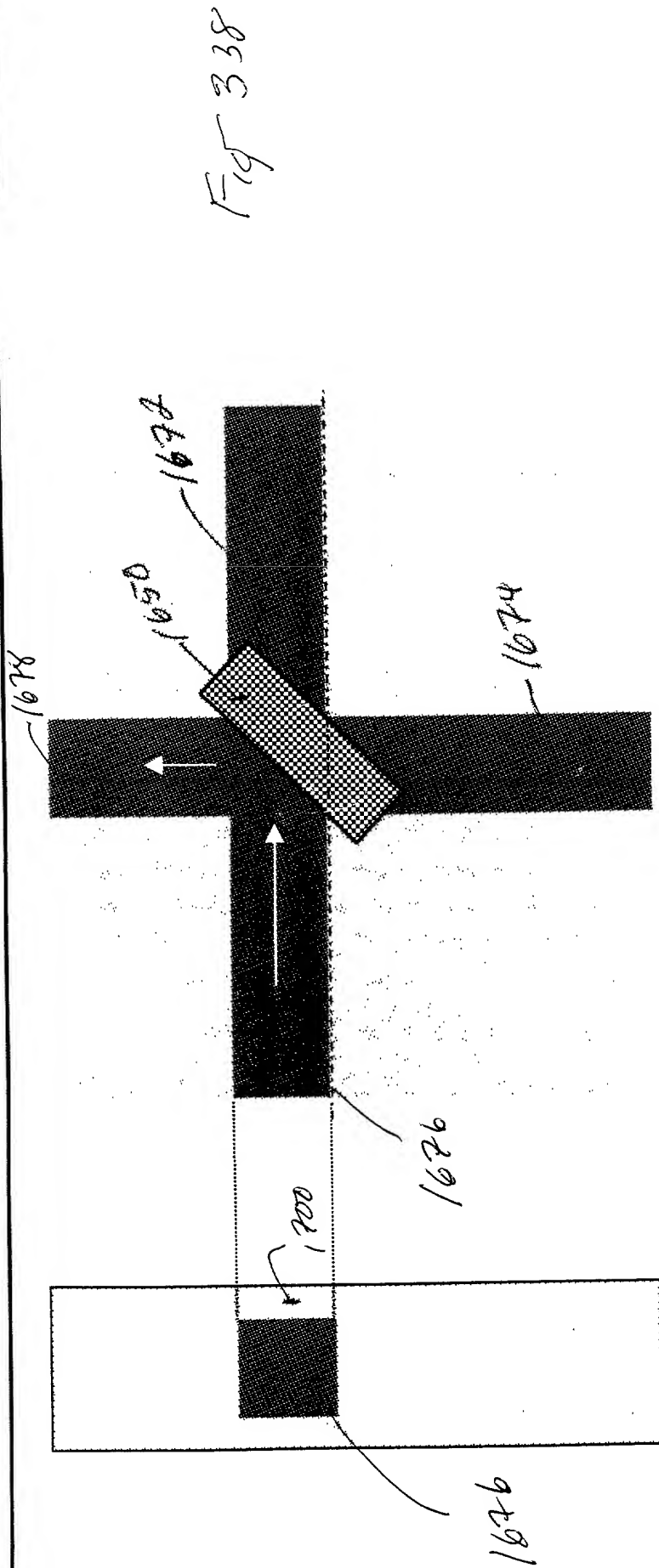


Fig. Add-9/23/99-3

# Conventional Corner Turning Structure

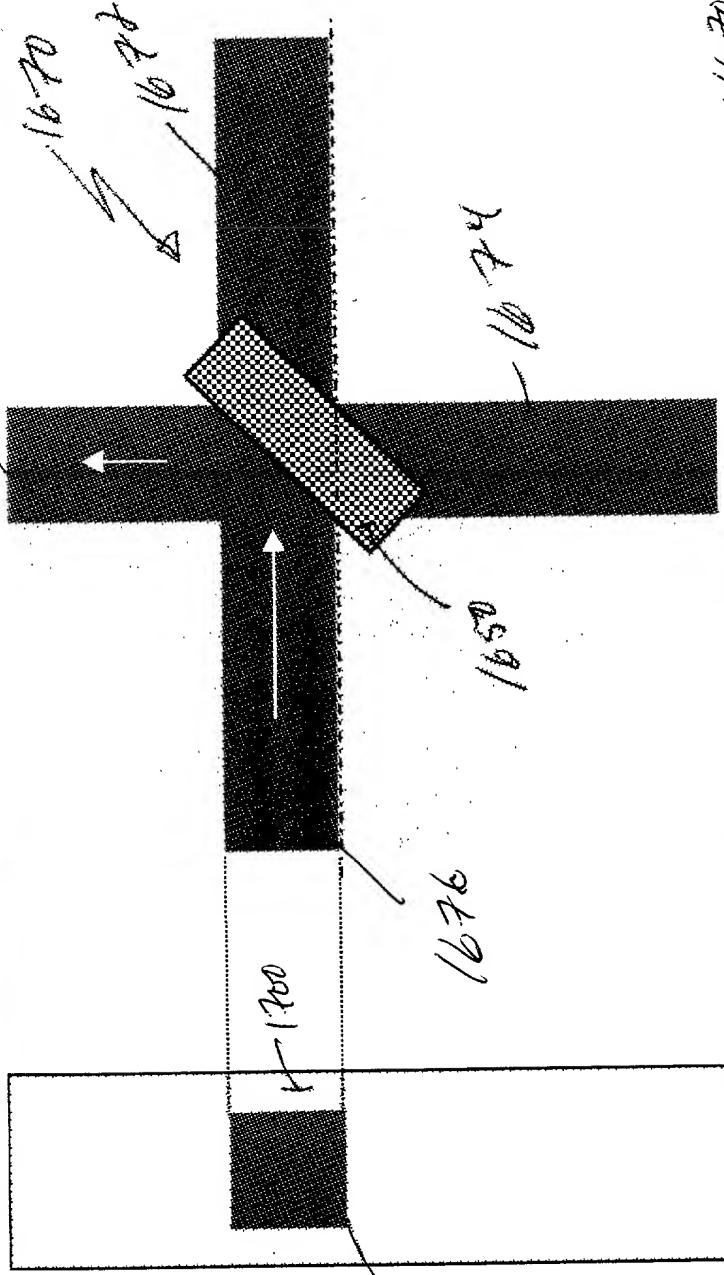


Fig 336  
1676

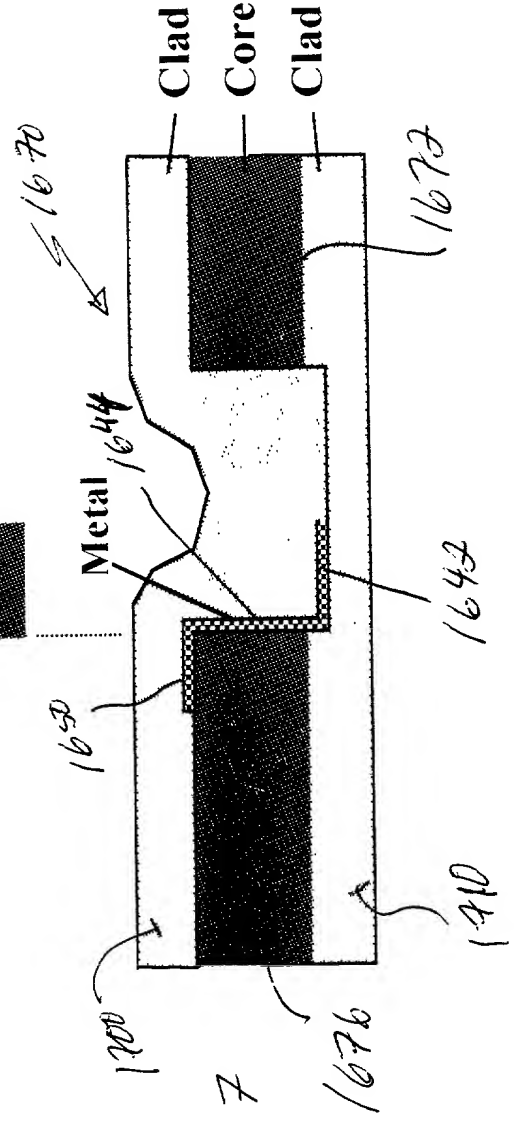
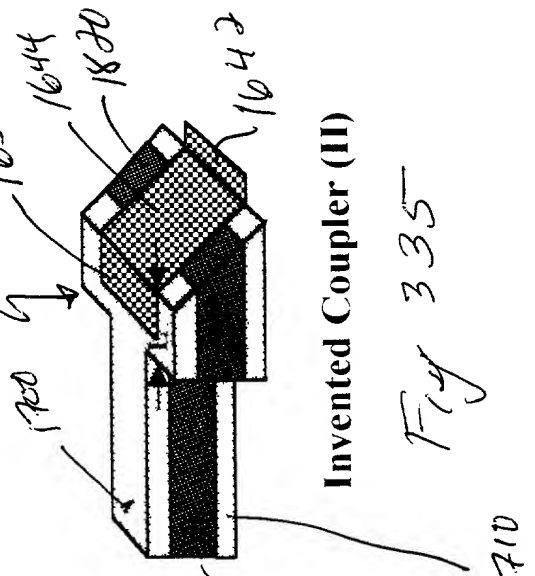
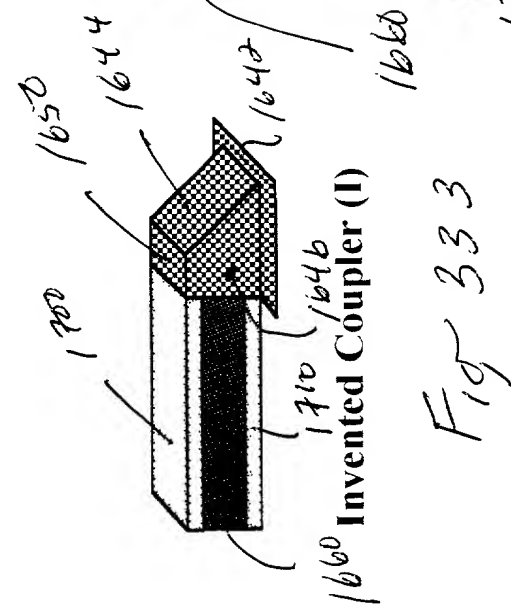
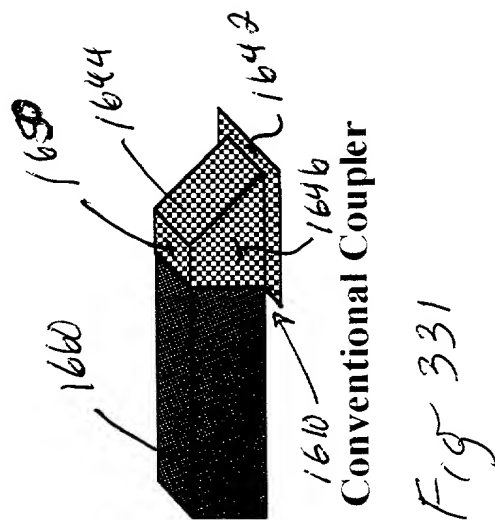
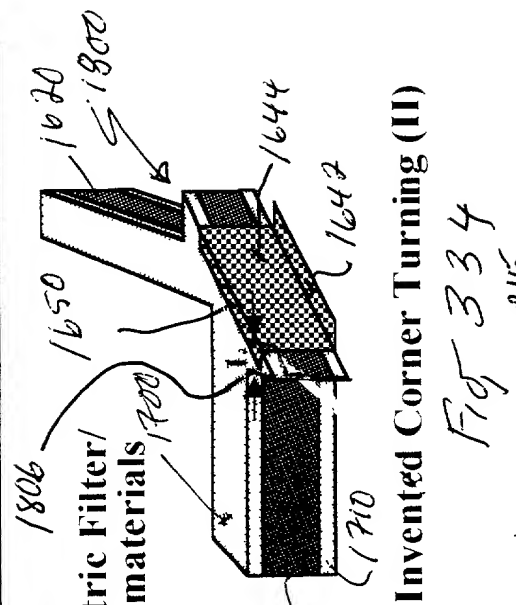
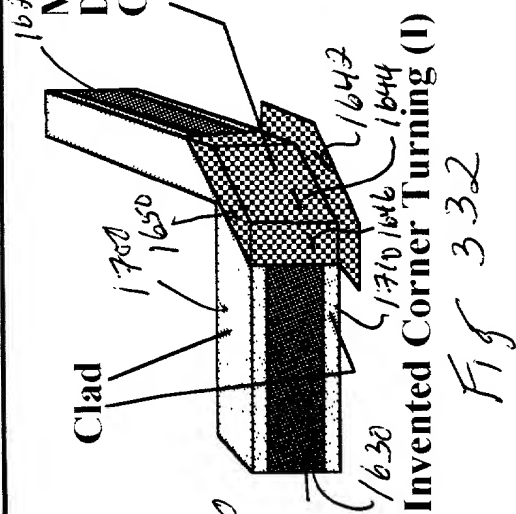
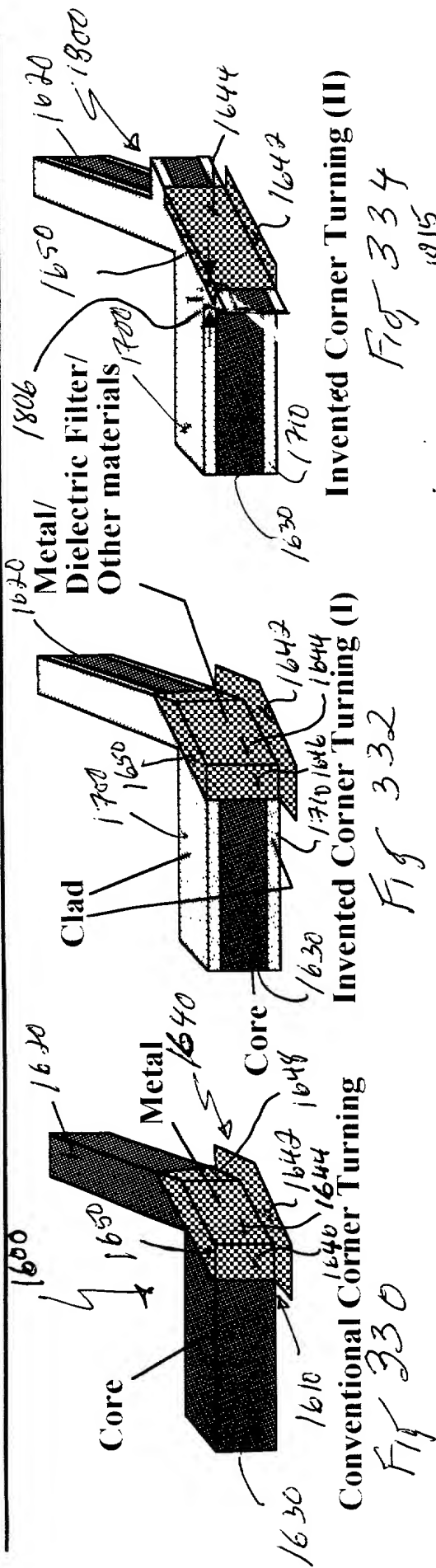


Fig 337

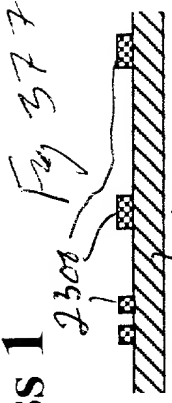
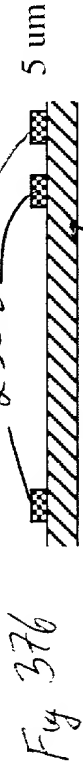
# Conventional and Invented Waveguide Structure Examples





# Example 3: Z waveguide Fab. Process 1

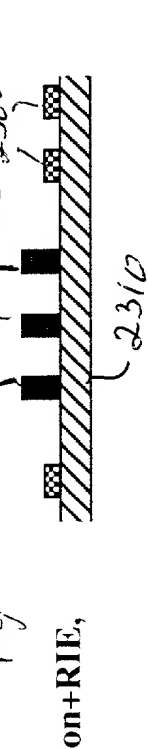
(a1) Metal pattern formation



(a2) Core coat9



(a3) Z-WG core patterning



[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]

Development

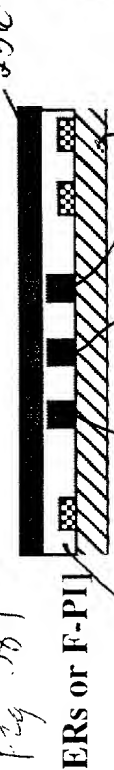
(for AlliedSig, ORMOCERS)

(a4) Clad coat



(for planarization viscosity adjust if necessary CMP)

(a5) Core coat



[DuPont, AlliedSig, ORMOCERS or F-PI]

(a6) WG core patterning



[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]

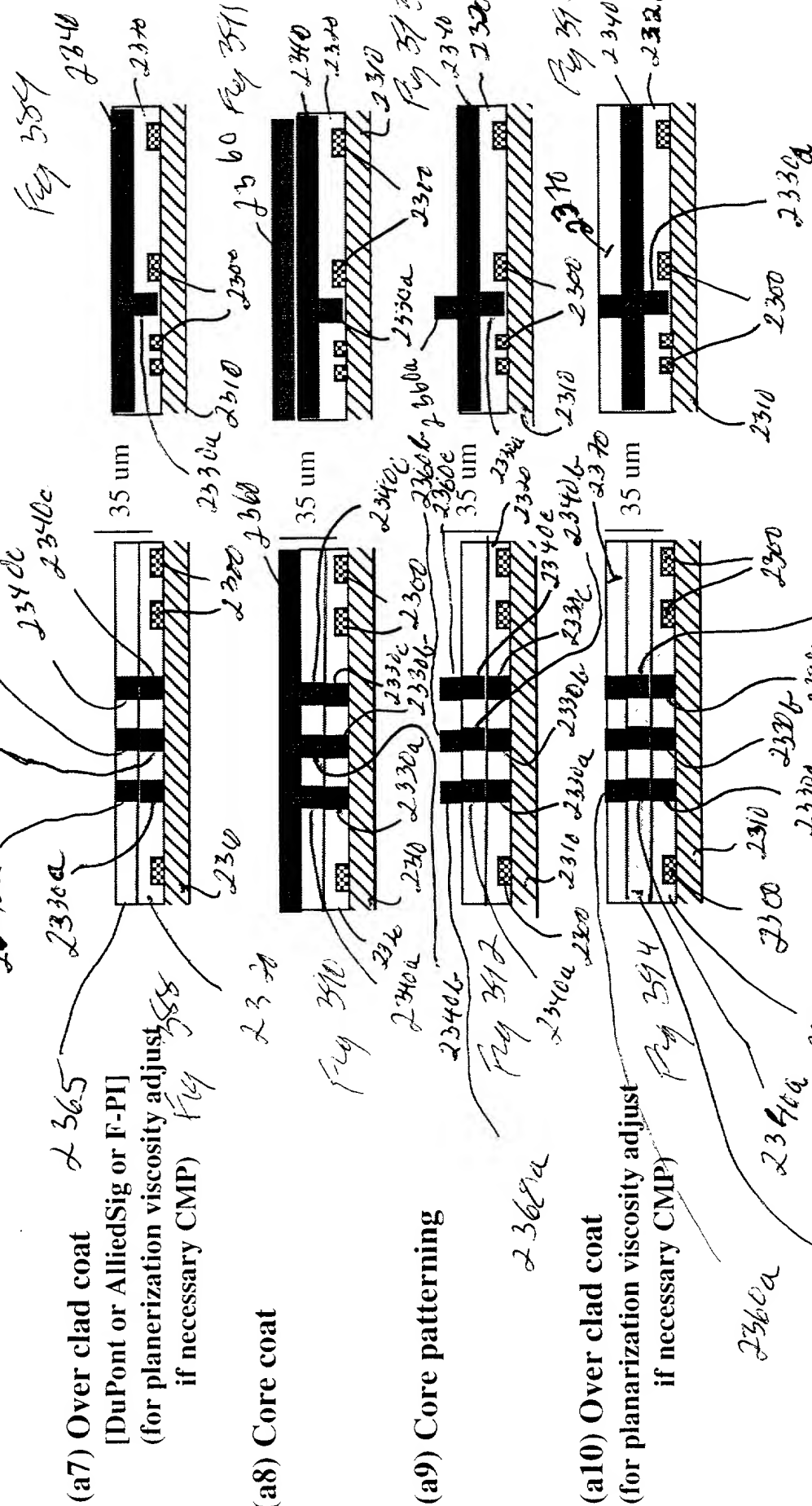
Development

(for AlliedSig, ORMOCERS)



Fig. 16-1

2330a



In the case of multi layer (a1-a10) or (a2-a10) process is repeated on the (a10).

2365

Fig. 16-2

# Example 4: Z waveguide Fab. Process 2

(a1) Metal pattern formation

Fig 396

(a2) Clad coat

[DuPont, AlliedSig, ORMOCERs or F-PI]

(a3) Clad patterning

Fig 398

[UV-Exposure, mask-formation+RIE,

Laser or Dupont process]

Development

(for AlliedSig, ORMOCERs)

(a4) Core coat

(for planarization viscosity adjust

if necessary CMP)

Fig 402

(a5) WG core patterning

[UV-Exposure, mask-formation+RIE,

Laser or Dupont process]

Development

(for AlliedSig, ORMOCERs)

Fig 404

(a6) Over clad coat

[DuPont or AlliedSig or F-PI]

(for planarization viscosity adjust

if necessary CMP)

Fig 406

Fig 397

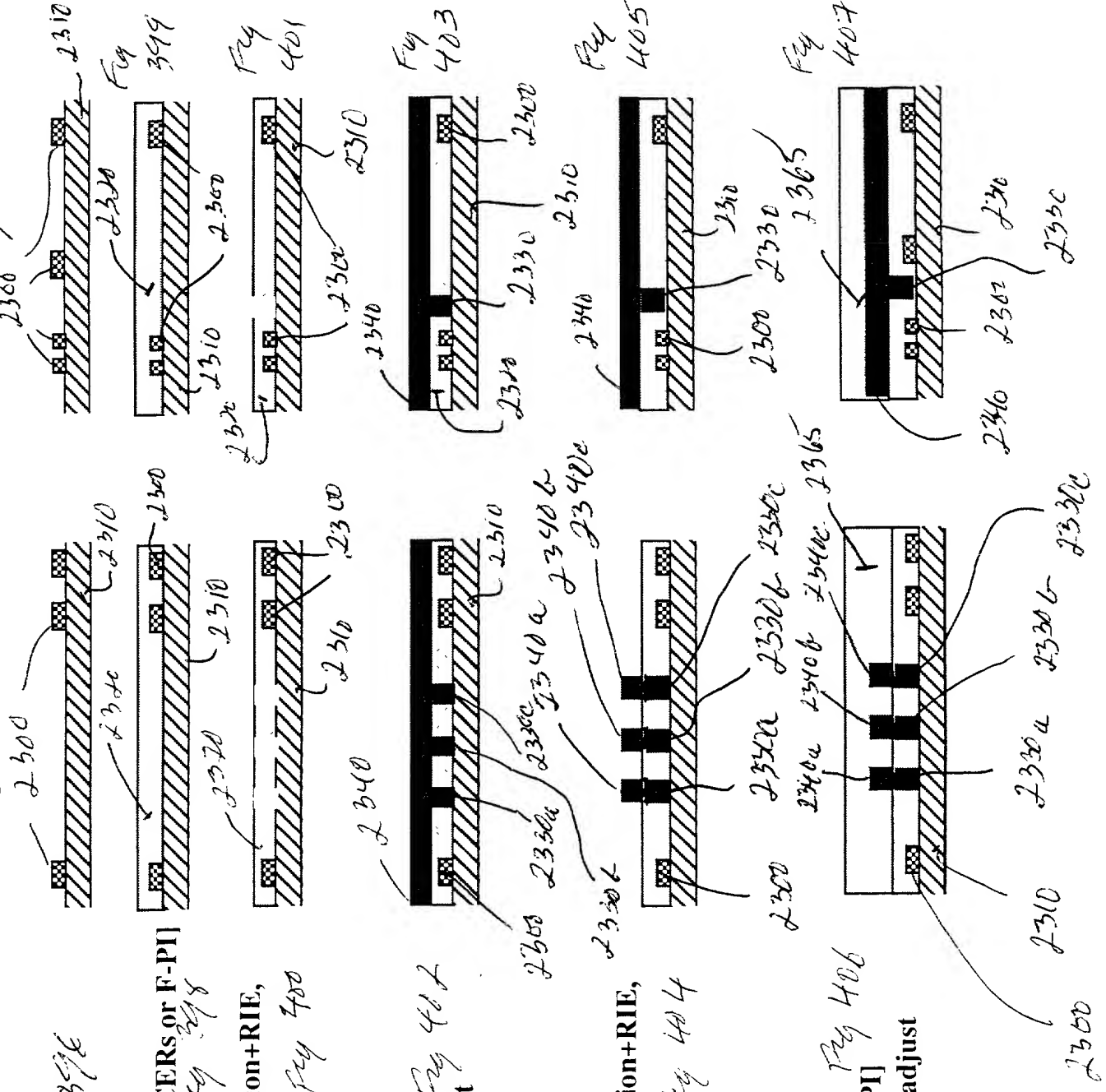
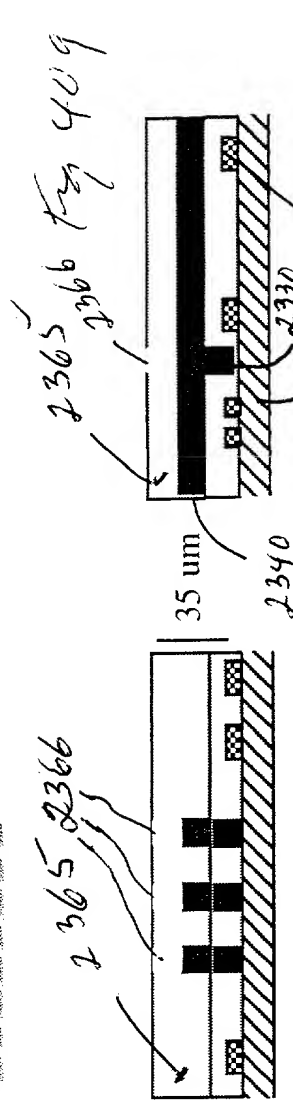


Fig. 17-1

(a7) Clad patterning

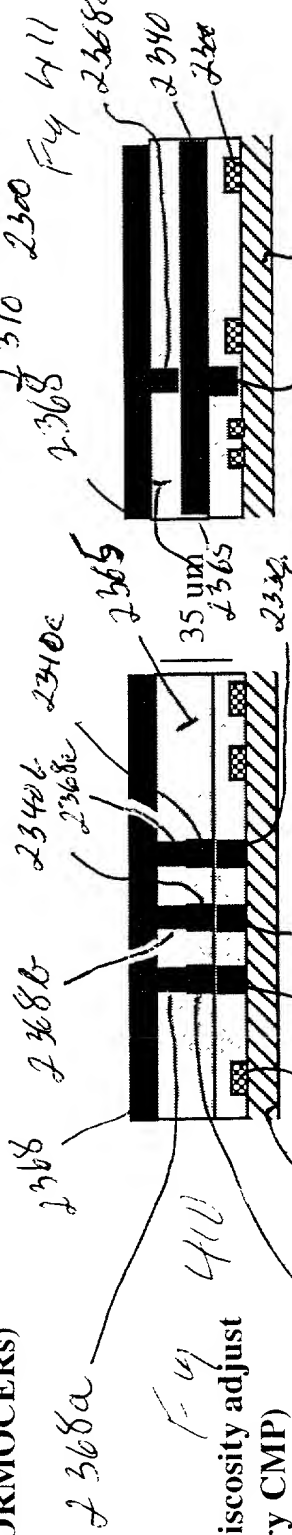
[UV-Exposure, mask-formation+RIE,  
Laser or Dupont process] Fig 408  
Development

(for AlliedSig, ORMOCERs)



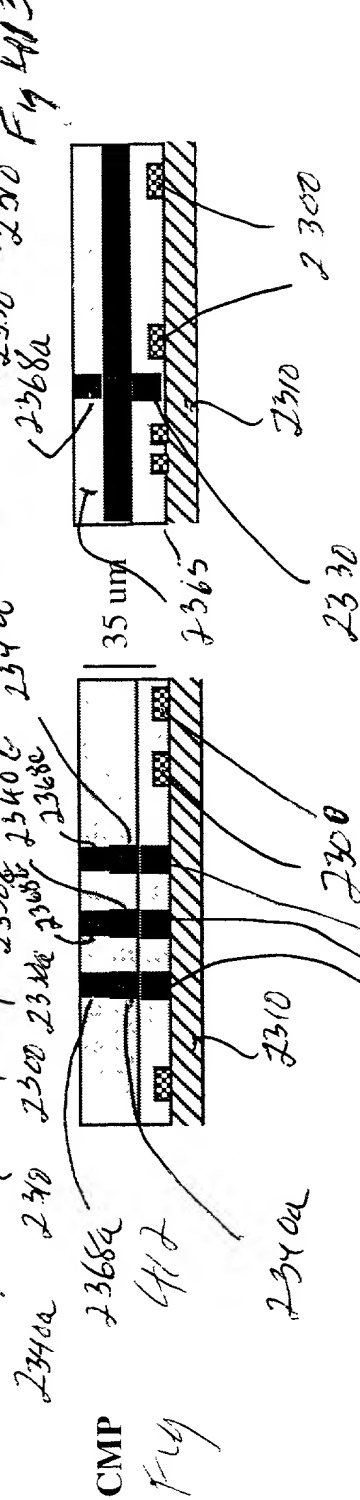
(a8) Core coat

(for planarization viscosity adjust  
if necessary CMP)



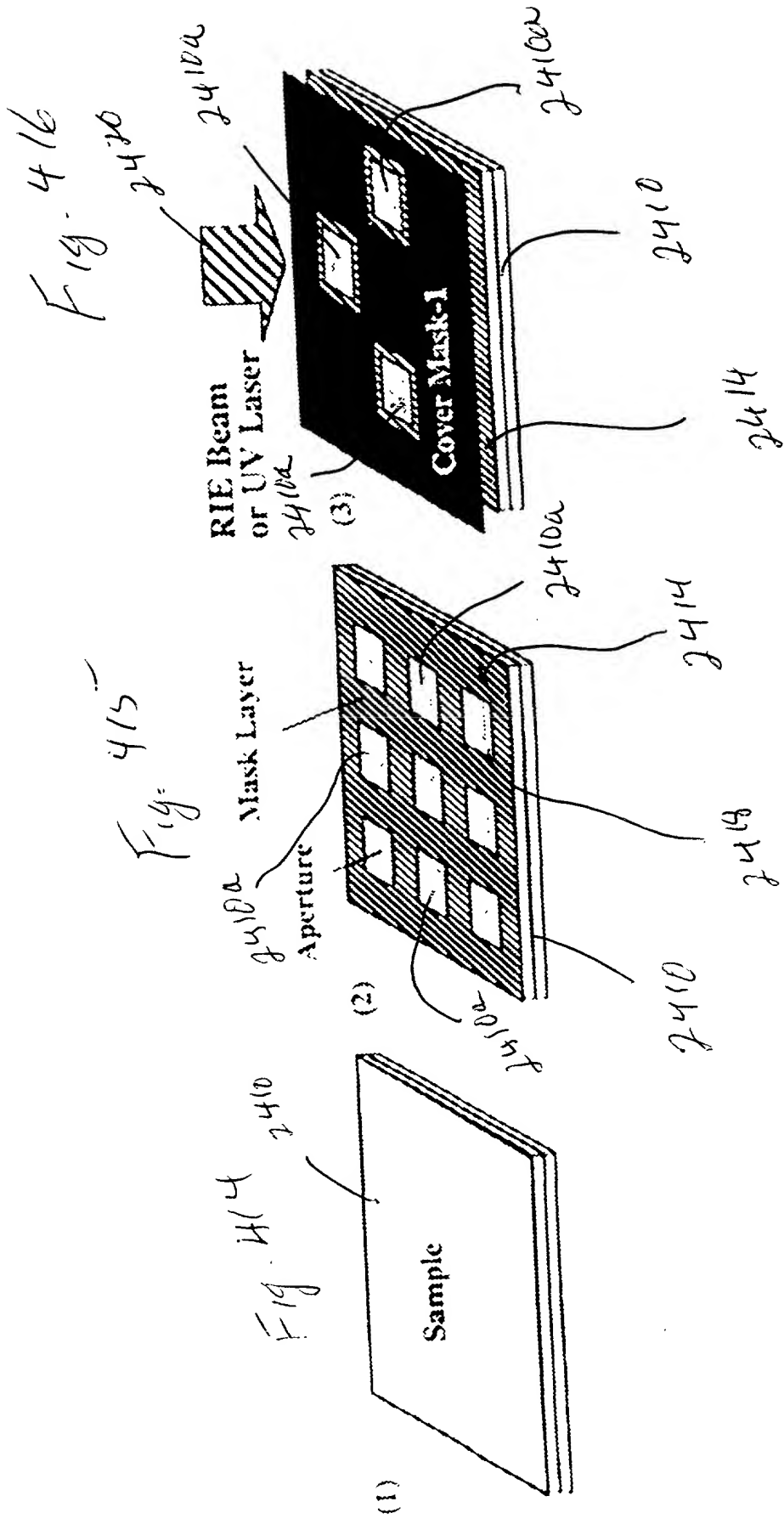
or

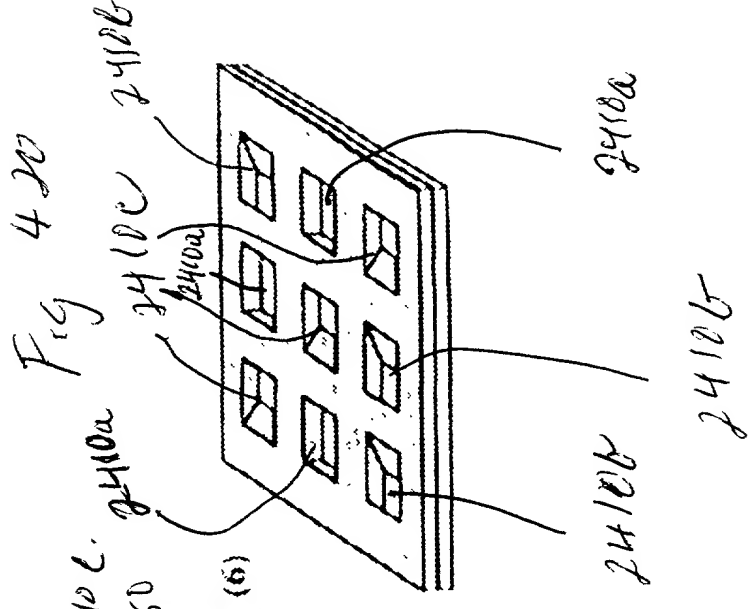
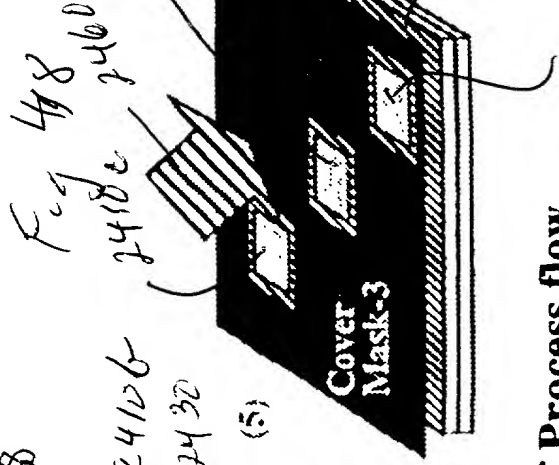
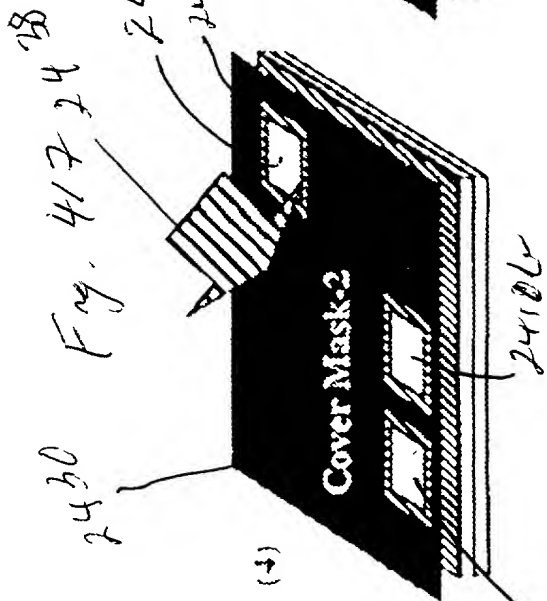
(a8) Core coat and CMP



In the case of multi layer (a1, a5-a8) or (a5-a8) process is repeated on the (a8).

Fig. 17-2

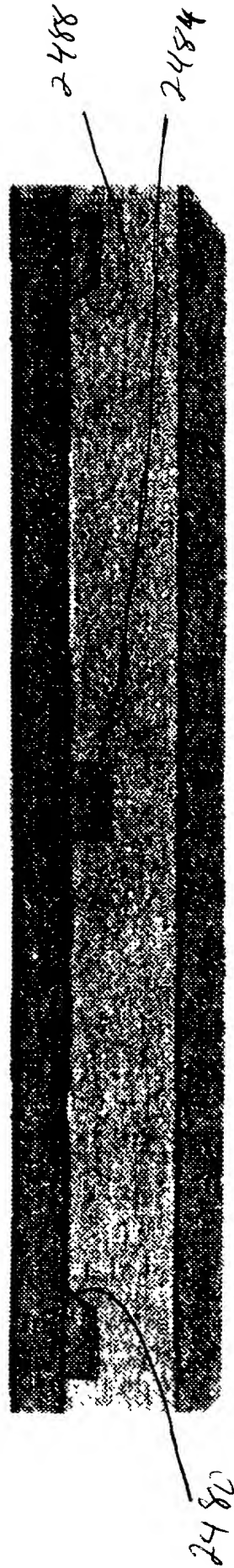




(a) Conceptual illustration of Process flow

2410b

Fig. 4d1



(b) Trench wall formation of three different angles